NV3052CGRB
Application Notes

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Revision History

Version No.	Data	Description
V0.1	2020/05/19	New

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1. BOE 4.2 Panel(GV042FBM-N80-1AP0)

```
=============== RGB Timing ===============
H Active = 720
H Back Porch (Sync Width Not Included) = 44
H Front Porch = 46
H Pulse Width = 2
V Active = 672
V Back Porch (Sync Width Not Included) = 14
V Front Porch = 16
V Pulse Width = 2
=============== initial code ===============
  //DCLK=35MHz

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x01);
Wrt_Reg_3052(0xE3,0x00);
Wrt_Reg_3052(0xF6,0xC0);
Wrt_Reg_3052(0xF0,0x00);
Wrt_Reg_3052(0x0A,0x01);
Wrt_Reg_3052(0x23,0xA0);
Wrt_Reg_3052(0x24,0x10);
Wrt_Reg_3052(0x25,0x10);
Wrt_Reg_3052(0x26,0x2E);
Wrt_Reg_3052(0x27,0x2E);
Wrt_Reg_3052(0x29,0x02);
Wrt_Reg_3052(0x2A,0x9F);
Wrt_Reg_3052(0x32,0x34);
Wrt_Reg_3052(0x38,0x9C);
Wrt_Reg_3052(0x39,0xA7);
Wrt_Reg_3052(0x3A,0x3f);
Wrt_Reg_3052(0x3B,0x94);
Wrt_Reg_3052(0x40,0x07);
Wrt_Reg_3052(0x42,0x6D);
Wrt_Reg_3052(0x43,0x83);
Wrt_Reg_3052(0x81,0x00);
Wrt_Reg_3052(0x91,0x77);
Wrt_Reg_3052(0x92,0x77);

Wrt_Reg_3052(0xA0,0x52);
Wrt_Reg_3052(0xA1,0x50);
Wrt_Reg_3052(0xA4,0x9C);
Wrt_Reg_3052(0xA7,0x02);
Wrt_Reg_3052(0xA8,0x02);
Wrt_Reg_3052(0xA9,0x02);
Wrt_Reg_3052(0xAA,0xA8);
Wrt_Reg_3052(0xAB,0x28);
Wrt_Reg_3052(0xAE,0xD2);
Wrt_Reg_3052(0xAF,0x02);
Wrt_Reg_3052(0xB0,0xD2);
Wrt_Reg_3052(0xB2,0x26);
Wrt_Reg_3052(0xB3,0x26);

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x02);
```

```
Wrt_Reg_3052(0xB0,0x02);
Wrt_Reg_3052(0xB1,0x10);
Wrt_Reg_3052(0xB2,0x0E);
Wrt_Reg_3052(0xB3,0x35);
Wrt_Reg_3052(0xB4,0x37);
Wrt_Reg_3052(0xB5,0x3C);
Wrt_Reg_3052(0xB6,0x1A);
Wrt_Reg_3052(0xB7,0x38);
Wrt_Reg_3052(0xB8,0x0E);
Wrt_Reg_3052(0xB9,0x05);
Wrt_Reg_3052(0xBA,0x11);
Wrt_Reg_3052(0xBB,0x11);
Wrt_Reg_3052(0xBC,0x13);
Wrt_Reg_3052(0xBD,0x14);
Wrt_Reg_3052(0xBE,0x16);
Wrt_Reg_3052(0xBF,0x0C);
Wrt_Reg_3052(0xC0,0x17);
Wrt_Reg_3052(0xC1,0x06);
Wrt_Reg_3052(0xD0,0x02);
Wrt_Reg_3052(0xD1,0x10);
Wrt_Reg_3052(0xD2,0x0E);
Wrt_Reg_3052(0xD3,0x35);
Wrt_Reg_3052(0xD4,0x37);
Wrt_Reg_3052(0xD5,0x3C);
Wrt_Reg_3052(0xD6,0x1A);
Wrt_Reg_3052(0xD7,0x39);
Wrt_Reg_3052(0xD8,0x0E);
Wrt_Reg_3052(0xD9,0x05);
Wrt_Reg_3052(0xDA,0x11);
Wrt_Reg_3052(0xDB,0x11);
Wrt_Reg_3052(0xDC,0x13);
Wrt_Reg_3052(0xDD,0x14);
Wrt_Reg_3052(0xDE,0x16);
Wrt_Reg_3052(0xDF,0x0C);
Wrt_Reg_3052(0xE0,0x17);
Wrt_Reg_3052(0xE1,0x06);
Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x03);
Wrt_Reg_3052(0x00,0x2A);
Wrt_Reg_3052(0x01,0x2A);
Wrt_Reg_3052(0x02,0x2A);
Wrt_Reg_3052(0x03,0x2A);
Wrt_Reg_3052(0x04,0x81);
Wrt_Reg_3052(0x06,0x26);
Wrt_Reg_3052(0x07,0x02);
Wrt_Reg_3052(0x08,0x06);
Wrt_Reg_3052(0x09,0x07);
Wrt_Reg_3052(0x0A,0x08);
Wrt_Reg_3052(0x0B,0x09);
Wrt_Reg_3052(0x20,0x2A);
Wrt_Reg_3052(0x21,0x2A);
Wrt_Reg_3052(0x22,0x2A);
Wrt_Reg_3052(0x23,0x2A);
Wrt_Reg_3052(0x24,0x81);
Wrt_Reg_3052(0x26,0x26);
Wrt_Reg_3052(0x27,0x02);
```

```
Wrt_Reg_3052(0x28,0x00);
Wrt_Reg_3052(0x2A,0x02);
Wrt_Reg_3052(0x2B,0x02);
Wrt_Reg_3052(0x70,0x32);
Wrt_Reg_3052(0x71,0x00);
Wrt_Reg_3052(0x30,0x2A);
Wrt_Reg_3052(0x31,0x2A);
Wrt_Reg_3052(0x32,0x2A);
Wrt_Reg_3052(0x33,0x2A);
Wrt_Reg_3052(0x34,0x81);
Wrt_Reg_3052(0x35,0x26);
Wrt_Reg_3052(0x37,0x13);
Wrt_Reg_3052(0x40,0x09);
Wrt_Reg_3052(0x41,0x0A);
Wrt_Reg_3052(0x42,0x0B);
Wrt_Reg_3052(0x43,0x0C);
Wrt_Reg_3052(0x44,0x22);
Wrt_Reg_3052(0x45,0xB1);
Wrt_Reg_3052(0x46,0xB2);
Wrt_Reg_3052(0x47,0x22);
Wrt_Reg_3052(0x48,0xB3);
Wrt_Reg_3052(0x49,0xB4);
Wrt_Reg_3052(0x50,0x0D);
Wrt_Reg_3052(0x51,0x0E);
Wrt_Reg_3052(0x52,0x0F);
Wrt_Reg_3052(0x53,0x10);
Wrt_Reg_3052(0x54,0x22);
Wrt_Reg_3052(0x55,0xB5);
Wrt_Reg_3052(0x56,0xB6);
Wrt_Reg_3052(0x57,0x22);
Wrt_Reg_3052(0x58,0xB7);
Wrt_Reg_3052(0x59,0xB8);
Wrt_Reg_3052(0x80,0x00);
Wrt_Reg_3052(0x81,0x1F);
Wrt_Reg_3052(0x82,0x00);
Wrt_Reg_3052(0x83,0x06);
Wrt_Reg_3052(0x84,0x0E);
Wrt_Reg_3052(0x85,0x10);
Wrt_Reg_3052(0x86,0x0A);
Wrt_Reg_3052(0x87,0x0C);
Wrt_Reg_3052(0x88,0x00);
Wrt_Reg_3052(0x89,0x1F);
Wrt_Reg_3052(0x8A,0x02);
Wrt_Reg_3052(0x8B,0x04);
Wrt_Reg_3052(0x96,0x00);
Wrt_Reg_3052(0x97,0x1F);
Wrt_Reg_3052(0x98,0x00);
Wrt_Reg_3052(0x99,0x05);
Wrt_Reg_3052(0x9A,0x0D);
Wrt_Reg_3052(0x9B,0x0F);
Wrt_Reg_3052(0x9C,0x09);
Wrt_Reg_3052(0x9D,0x0B);
Wrt_Reg_3052(0x9E,0x00);
Wrt_Reg_3052(0x9F,0x1F);
Wrt_Reg_3052(0xA0,0x01);
Wrt_Reg_3052(0xA1,0x03);
Wrt_Reg_3052(0xB0,0x1F);
```

```
Wrt_Reg_3052(0xB1,0x00);
Wrt_Reg_3052(0xB2,0x00);
Wrt_Reg_3052(0xB3,0x06);
Wrt_Reg_3052(0xB4,0x0B);
Wrt_Reg_3052(0xB5,0x09);
Wrt_Reg_3052(0xB6,0x0F);
Wrt_Reg_3052(0xB7,0x0D);
Wrt_Reg_3052(0xB8,0x00);
Wrt_Reg_3052(0xB9,0x1F);
Wrt_Reg_3052(0xBA,0x03);
Wrt_Reg_3052(0xBB,0x01);
Wrt_Reg_3052(0xC6,0x1F);
Wrt_Reg_3052(0xC7,0x00);
Wrt_Reg_3052(0xC8,0x00);
Wrt_Reg_3052(0xC9,0x05);
Wrt_Reg_3052(0xCA,0x0C);
Wrt_Reg_3052(0xCB,0x0A);
Wrt_Reg_3052(0xCC,0x10);
Wrt_Reg_3052(0xCD,0x0E);
Wrt_Reg_3052(0xCE,0x00);
Wrt_Reg_3052(0xCF,0x1F);
Wrt_Reg_3052(0xD0,0x04);
Wrt_Reg_3052(0xD1,0x02);

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x00);
Wrt_Reg_3052(0x3a,0x66);
Wrt_Reg_3052(0x36,0x02);//0x01

Wrt_Reg_3052(0x11,0x00);
Delay_ms(200);
Wrt_Reg_3052(0x29,0x00);
Delay_ms(10);
```

2. CTC3.45 Panel (ZH035IA-01A)

```
=============== RGB Timing ===============
H Active = 640
H Back Porch (Sync Width Not Included) = 20
H Front Porch = 20
H Pulse Width = 2
V Active = 480
V Back Porch (Sync Width Not Included) = 4
V Front Porch = 12
V Pulse Width = 2
=============== initial code===============
    //正扫   DCLK=20MHz

    Wrt_Reg_3052(0xFF,0x30);
    Wrt_Reg_3052(0xFF,0x52);
    Wrt_Reg_3052(0xFF,0x01);
    Wrt_Reg_3052(0xE3,0x00);
    Wrt_Reg_3052(0x40,0x00);
    Wrt_Reg_3052(0x03,0x40);
    Wrt_Reg_3052(0x04,0x00);
    Wrt_Reg_3052(0x05,0x03);
```

```
Wrt_Reg_3052(0x08,0x00);
Wrt_Reg_3052(0x09,0x07);
Wrt_Reg_3052(0x0A,0x01);
Wrt_Reg_3052(0x0B,0x32);
Wrt_Reg_3052(0x0C,0x32);
Wrt_Reg_3052(0x0D,0x0B);
Wrt_Reg_3052(0x0E,0x00);
Wrt_Reg_3052(0x23,0xA2);

Wrt_Reg_3052(0x24,0x0c);
Wrt_Reg_3052(0x25,0x06);
Wrt_Reg_3052(0x26,0x14);
Wrt_Reg_3052(0x27,0x14);

Wrt_Reg_3052(0x38,0x9C);
Wrt_Reg_3052(0x39,0xA7);
Wrt_Reg_3052(0x3A,0x47);

Wrt_Reg_3052(0x28,0x40);
Wrt_Reg_3052(0x29,0x01);
Wrt_Reg_3052(0x2A,0xdf);
Wrt_Reg_3052(0x49,0x3C);
Wrt_Reg_3052(0x91,0x57);
Wrt_Reg_3052(0x92,0x57);
Wrt_Reg_3052(0xA0,0x55);
Wrt_Reg_3052(0xA1,0x50);
Wrt_Reg_3052(0xA4,0x9C);
Wrt_Reg_3052(0xA7,0x02);
Wrt_Reg_3052(0xA8,0x01);
Wrt_Reg_3052(0xA9,0x01);
Wrt_Reg_3052(0xAA,0xFC);
Wrt_Reg_3052(0xAB,0x28);
Wrt_Reg_3052(0xAC,0x06);
Wrt_Reg_3052(0xAD,0x06);
Wrt_Reg_3052(0xAE,0x06);
Wrt_Reg_3052(0xAF,0x03);
Wrt_Reg_3052(0xB0,0x08);
Wrt_Reg_3052(0xB1,0x26);
Wrt_Reg_3052(0xB2,0x28);
Wrt_Reg_3052(0xB3,0x28);
Wrt_Reg_3052(0xB4,0x03);
Wrt_Reg_3052(0xB5,0x08);
Wrt_Reg_3052(0xB6,0x26);
Wrt_Reg_3052(0xB7,0x08);
Wrt_Reg_3052(0xB8,0x26);
Wrt_Reg_3052(0xF0,0x00);
Wrt_Reg_3052(0xF6,0xC0);


Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x02);
Wrt_Reg_3052(0xB0,0x0B);
Wrt_Reg_3052(0xB1,0x16);
Wrt_Reg_3052(0xB2,0x17);
Wrt_Reg_3052(0xB3,0x2C);
Wrt_Reg_3052(0xB4,0x32);
```

```
Wrt_Reg_3052(0xB5,0x3B);
Wrt_Reg_3052(0xB6,0x29);
Wrt_Reg_3052(0xB7,0x40);
Wrt_Reg_3052(0xB8,0x0d);
Wrt_Reg_3052(0xB9,0x05);
Wrt_Reg_3052(0xBA,0x12);
Wrt_Reg_3052(0xBB,0x10);
Wrt_Reg_3052(0xBC,0x12);
Wrt_Reg_3052(0xBD,0x15);
Wrt_Reg_3052(0xBE,0x19);
Wrt_Reg_3052(0xBF,0x0E);
Wrt_Reg_3052(0xC0,0x16);
Wrt_Reg_3052(0xC1,0x0A);
Wrt_Reg_3052(0xD0,0x0C);
Wrt_Reg_3052(0xD1,0x17);
Wrt_Reg_3052(0xD2,0x14);
Wrt_Reg_3052(0xD3,0x2E);
Wrt_Reg_3052(0xD4,0x32);
Wrt_Reg_3052(0xD5,0x3C);
Wrt_Reg_3052(0xD6,0x22);
Wrt_Reg_3052(0xD7,0x3D);
Wrt_Reg_3052(0xD8,0x0D);
Wrt_Reg_3052(0xD9,0x07);
Wrt_Reg_3052(0xDA,0x13);
Wrt_Reg_3052(0xDB,0x13);
Wrt_Reg_3052(0xDC,0x11);
Wrt_Reg_3052(0xDD,0x15);
Wrt_Reg_3052(0xDE,0x19);
Wrt_Reg_3052(0xDF,0x10);
Wrt_Reg_3052(0xE0,0x17);
Wrt_Reg_3052(0xE1,0x0A);
Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x03);
Wrt_Reg_3052(0x00,0x2A);
Wrt_Reg_3052(0x01,0x2A);
Wrt_Reg_3052(0x02,0x2A);
Wrt_Reg_3052(0x03,0x2A);
Wrt_Reg_3052(0x04,0x61);
Wrt_Reg_3052(0x05,0x80);
Wrt_Reg_3052(0x06,0xc7);
Wrt_Reg_3052(0x07,0x01);
Wrt_Reg_3052(0x08,0x03);
Wrt_Reg_3052(0x09,0x04);
Wrt_Reg_3052(0x70,0x22);
Wrt_Reg_3052(0x71,0x80);
Wrt_Reg_3052(0x30,0x2A);
Wrt_Reg_3052(0x31,0x2A);
Wrt_Reg_3052(0x32,0x2A);
Wrt_Reg_3052(0x33,0x2A);
Wrt_Reg_3052(0x34,0x61);
Wrt_Reg_3052(0x35,0xc5);
Wrt_Reg_3052(0x36,0x80);
Wrt_Reg_3052(0x37,0x23);
Wrt_Reg_3052(0x40,0x03);
Wrt_Reg_3052(0x41,0x04);
Wrt_Reg_3052(0x42,0x05);
```

```
Wrt_Reg_3052(0x43,0x06);
Wrt_Reg_3052(0x44,0x11);
Wrt_Reg_3052(0x45,0xe8);
Wrt_Reg_3052(0x46,0xe9);
Wrt_Reg_3052(0x47,0x11);
Wrt_Reg_3052(0x48,0xea);
Wrt_Reg_3052(0x49,0xeb);
Wrt_Reg_3052(0x50,0x07);
Wrt_Reg_3052(0x51,0x08);
Wrt_Reg_3052(0x52,0x09);
Wrt_Reg_3052(0x53,0x0a);
Wrt_Reg_3052(0x54,0x11);
Wrt_Reg_3052(0x55,0xec);
Wrt_Reg_3052(0x56,0xed);
Wrt_Reg_3052(0x57,0x11);
Wrt_Reg_3052(0x58,0xef);
Wrt_Reg_3052(0x59,0xf0);
Wrt_Reg_3052(0xB1,0x01);
Wrt_Reg_3052(0xB4,0x15);
Wrt_Reg_3052(0xB5,0x16);
Wrt_Reg_3052(0xB6,0x09);
Wrt_Reg_3052(0xB7,0x0f);
Wrt_Reg_3052(0xB8,0x0d);
Wrt_Reg_3052(0xB9,0x0b);
Wrt_Reg_3052(0xBA,0x00);
Wrt_Reg_3052(0xC7,0x02);
Wrt_Reg_3052(0xCA,0x17);
Wrt_Reg_3052(0xCB,0x18);
Wrt_Reg_3052(0xCC,0x0a);
Wrt_Reg_3052(0xCD,0x10);
Wrt_Reg_3052(0xCE,0x0e);
Wrt_Reg_3052(0xCF,0x0c);
Wrt_Reg_3052(0xD0,0x00);
Wrt_Reg_3052(0x81,0x00);
Wrt_Reg_3052(0x84,0x15);
Wrt_Reg_3052(0x85,0x16);
Wrt_Reg_3052(0x86,0x10);
Wrt_Reg_3052(0x87,0x0a);
Wrt_Reg_3052(0x88,0x0c);
Wrt_Reg_3052(0x89,0x0e);
Wrt_Reg_3052(0x8A,0x02);
Wrt_Reg_3052(0x97,0x00);
Wrt_Reg_3052(0x9A,0x17);
Wrt_Reg_3052(0x9B,0x18);
Wrt_Reg_3052(0x9C,0x0f);
Wrt_Reg_3052(0x9D,0x09);
Wrt_Reg_3052(0x9E,0x0b);
Wrt_Reg_3052(0x9F,0x0d);
Wrt_Reg_3052(0xA0,0x01);
Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x02);
Wrt_Reg_3052(0x01,0x01);
Wrt_Reg_3052(0x02,0xDA);
Wrt_Reg_3052(0x03,0xBA);
Wrt_Reg_3052(0x04,0xA8);
Wrt_Reg_3052(0x05,0x9A);
```

```
Wrt_Reg_3052(0x06,0x70);
Wrt_Reg_3052(0x07,0xFF);
Wrt_Reg_3052(0x08,0x91);
Wrt_Reg_3052(0x09,0x90);
Wrt_Reg_3052(0x0A,0xFF);
Wrt_Reg_3052(0x0B,0x8F);
Wrt_Reg_3052(0x0C,0x60);
Wrt_Reg_3052(0x0D,0x58);
Wrt_Reg_3052(0x0E,0x48);
Wrt_Reg_3052(0x0F,0x38);
Wrt_Reg_3052(0x10,0x2B);
Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x00);
Wrt_Reg_3052(0x36,0x0a);
Wrt_Reg_3052(0x11,0x00);
Delay_ms( 200 );
Wrt_Reg_3052(0x29,0x00);
Delay_ms(10);
```

3. CTC5 .99Panel (PH060IA-01B)

```
=============== RGB Timing ===============
H Active = 720
H Back Porch (Sync Width Not Included) = 30
H Front Porch = 24
H Pulse Width = 2
V Active =1440
V Back Porch (Sync Width Not Included) = 18
V Front Porch = 14
V Pulse Width = 2
=============== initial code===============
//正扫 DCLK=60~68MHz

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x01);
Wrt_Reg_3052(0xE3,0x00);

Wrt_Reg_3052(0x03,0x40);
Wrt_Reg_3052(0x04,0x00);
Wrt_Reg_3052(0x05,0x03);

Wrt_Reg_3052(0x08,0x00);
Wrt_Reg_3052(0x09,0x07);
Wrt_Reg_3052(0x0A,0x01);
Wrt_Reg_3052(0x0B,0x32);
Wrt_Reg_3052(0x0C,0x32);
Wrt_Reg_3052(0x0D,0x0B);
Wrt_Reg_3052(0x0E,0x00);
Wrt_Reg_3052(0x23,0xA2);
Wrt_Reg_3052(0x24,0x0E);
Wrt_Reg_3052(0x25,0x14);
Wrt_Reg_3052(0x29,0x05);
Wrt_Reg_3052(0x2A,0x9f);
Wrt_Reg_3052(0x38,0x9C);
Wrt_Reg_3052(0x39,0xA7);
```

```
Wrt_Reg_3052(0x3A,0x43);
Wrt_Reg_3052(0x41,0x57);
Wrt_Reg_3052(0x49,0x3C);
Wrt_Reg_3052(0x6D,0x00);
Wrt_Reg_3052(0x6E,0x00);
Wrt_Reg_3052(0x91,0x77);
Wrt_Reg_3052(0x92,0x77);
Wrt_Reg_3052(0x99,0x54);
Wrt_Reg_3052(0x9B,0x56);

Wrt_Reg_3052(0xA0,0x55);
Wrt_Reg_3052(0xA1,0x50);
Wrt_Reg_3052(0xA4,0x9C);
Wrt_Reg_3052(0xA7,0x02);
Wrt_Reg_3052(0xA8,0x01);
Wrt_Reg_3052(0xA9,0x01);
Wrt_Reg_3052(0xA7,0x02);
Wrt_Reg_3052(0xA8,0x01);
Wrt_Reg_3052(0xA9,0x01);
Wrt_Reg_3052(0xAA,0xA8);
Wrt_Reg_3052(0xAB,0x28);
Wrt_Reg_3052(0xAC,0xE0);
Wrt_Reg_3052(0xAD,0xE2);
Wrt_Reg_3052(0xAE,0xE2);
Wrt_Reg_3052(0xAF,0x02);
Wrt_Reg_3052(0xB0,0xE2);
Wrt_Reg_3052(0xB1,0x26);
Wrt_Reg_3052(0xB2,0x28);
Wrt_Reg_3052(0xB3,0x28);
Wrt_Reg_3052(0xB4,0x22);
Wrt_Reg_3052(0xB5,0xE2);
Wrt_Reg_3052(0xB6,0x26);
Wrt_Reg_3052(0xB7,0xE2);
Wrt_Reg_3052(0xB8,0x26);
Wrt_Reg_3052(0xF0,0x00);
Wrt_Reg_3052(0xF6,0xC0);

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x02);
Wrt_Reg_3052(0xB1,0x15);
Wrt_Reg_3052(0xD1,0x0B);
Wrt_Reg_3052(0xB4,0x2E);
Wrt_Reg_3052(0xD4,0x38);
Wrt_Reg_3052(0xB2,0x18);
Wrt_Reg_3052(0xD2,0x0E);
Wrt_Reg_3052(0xB3,0x37);
Wrt_Reg_3052(0xD3,0x31);
Wrt_Reg_3052(0xB6,0x28);
Wrt_Reg_3052(0xD6,0x24);
Wrt_Reg_3052(0xB7,0x41);
Wrt_Reg_3052(0xD7,0x3F);
Wrt_Reg_3052(0xC1,0x08);
Wrt_Reg_3052(0xE1,0x08);
Wrt_Reg_3052(0xB8,0x0E);
Wrt_Reg_3052(0xD8,0x0E);
Wrt_Reg_3052(0xB9,0x04);
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Wrt_Reg_3052(0xD9,0x06);
Wrt_Reg_3052(0xBD,0x13);
Wrt_Reg_3052(0xDD,0x13);
Wrt_Reg_3052(0xBC,0x11);
Wrt_Reg_3052(0xDC,0x11);
Wrt_Reg_3052(0xBB,0x0F);
Wrt_Reg_3052(0xDB,0x11);
Wrt_Reg_3052(0xBA,0x11);
Wrt_Reg_3052(0xDA,0x11);
Wrt_Reg_3052(0xBE,0x19);
Wrt_Reg_3052(0xDE,0x1B);
Wrt_Reg_3052(0xBF,0x0F);
Wrt_Reg_3052(0xDF,0x13);
Wrt_Reg_3052(0xC0,0x16);
Wrt_Reg_3052(0xE0,0x18);
Wrt_Reg_3052(0xB5,0x3A);
Wrt_Reg_3052(0xD5,0x37);
Wrt_Reg_3052(0xB0,0x02);
Wrt_Reg_3052(0xD0,0x05);

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x03);
Wrt_Reg_3052(0x00,0x2A);
Wrt_Reg_3052(0x01,0x2A);
Wrt_Reg_3052(0x02,0x2A);
Wrt_Reg_3052(0x03,0x2A);
Wrt_Reg_3052(0x04,0x81);
Wrt_Reg_3052(0x05,0x26);
Wrt_Reg_3052(0x07,0x00);
Wrt_Reg_3052(0x08,0x0C);
Wrt_Reg_3052(0x09,0x0D);
Wrt_Reg_3052(0x70,0x39);
Wrt_Reg_3052(0x71,0x00);
Wrt_Reg_3052(0x30,0x2A);
Wrt_Reg_3052(0x31,0x2A);
Wrt_Reg_3052(0x32,0x2A);
Wrt_Reg_3052(0x33,0x2A);
Wrt_Reg_3052(0x34,0x81);
Wrt_Reg_3052(0x35,0x26);
Wrt_Reg_3052(0x37,0x33);
Wrt_Reg_3052(0x40,0x0B);
Wrt_Reg_3052(0x41,0x0C);
Wrt_Reg_3052(0x42,0x0D);
Wrt_Reg_3052(0x43,0x0E);
Wrt_Reg_3052(0x45,0xB8);
Wrt_Reg_3052(0x46,0xB9);
Wrt_Reg_3052(0x48,0xBA);
Wrt_Reg_3052(0x49,0xBB);
Wrt_Reg_3052(0x50,0x0F);
Wrt_Reg_3052(0x51,0x10);
Wrt_Reg_3052(0x52,0x11);
Wrt_Reg_3052(0x53,0x12);
Wrt_Reg_3052(0x55,0xbc);
Wrt_Reg_3052(0x56,0xbd);
Wrt_Reg_3052(0x58,0xbe);
Wrt_Reg_3052(0x59,0xbf);
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Wrt_Reg_3052(0x80,0x10);
Wrt_Reg_3052(0x81,0x0e);
Wrt_Reg_3052(0x82,0x0c);
Wrt_Reg_3052(0x83,0x0a);
Wrt_Reg_3052(0x84,0x02);
Wrt_Reg_3052(0x85,0x00);
Wrt_Reg_3052(0x86,0x00);
Wrt_Reg_3052(0x87,0x00);
Wrt_Reg_3052(0x88,0x00);
Wrt_Reg_3052(0x92,0x15);
Wrt_Reg_3052(0x93,0x16);

Wrt_Reg_3052(0x96,0x0f);
Wrt_Reg_3052(0x97,0x0d);
Wrt_Reg_3052(0x98,0x0b);
Wrt_Reg_3052(0x99,0x09);
Wrt_Reg_3052(0x9A,0x01);
Wrt_Reg_3052(0x9B,0x00);
Wrt_Reg_3052(0x9C,0x00);
Wrt_Reg_3052(0x9D,0x00);
Wrt_Reg_3052(0x9E,0x00);
Wrt_Reg_3052(0xA8,0x17);
Wrt_Reg_3052(0xA9,0x18);

Wrt_Reg_3052(0xB0,0x0d);
Wrt_Reg_3052(0xB1,0x0f);
Wrt_Reg_3052(0xB2,0x09);
Wrt_Reg_3052(0xB3,0x0b);
Wrt_Reg_3052(0xB4,0x00);
Wrt_Reg_3052(0xB5,0x01);
Wrt_Reg_3052(0xB6,0x00);
Wrt_Reg_3052(0xB7,0x00);
Wrt_Reg_3052(0xB8,0x00);
Wrt_Reg_3052(0xC2,0x15);
Wrt_Reg_3052(0xC3,0x16);
Wrt_Reg_3052(0xC6,0x0e);
Wrt_Reg_3052(0xC7,0x10);
Wrt_Reg_3052(0xC8,0x0a);
Wrt_Reg_3052(0xC9,0x0c);
Wrt_Reg_3052(0xCA,0x00);
Wrt_Reg_3052(0xCB,0x02);
Wrt_Reg_3052(0xCC,0x00);
Wrt_Reg_3052(0xCD,0x00);
Wrt_Reg_3052(0xCE,0x00);
Wrt_Reg_3052(0xD8,0x17);
Wrt_Reg_3052(0xD9,0x18);

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x02);
Wrt_Reg_3052(0x01,0x01);
Wrt_Reg_3052(0x02,0xDA);
Wrt_Reg_3052(0x03,0xBA);
Wrt_Reg_3052(0x04,0xA8);
Wrt_Reg_3052(0x05,0x9A);
Wrt_Reg_3052(0x06,0x70);
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```
Wrt_Reg_3052(0x07,0xFF);
Wrt_Reg_3052(0x08,0x91);
Wrt_Reg_3052(0x09,0x90);
Wrt_Reg_3052(0x0A,0xFF);
Wrt_Reg_3052(0x0B,0x8F);
Wrt_Reg_3052(0x0C,0x60);
Wrt_Reg_3052(0x0D,0x58);
Wrt_Reg_3052(0x0E,0x48);
Wrt_Reg_3052(0x0F,0x38);
Wrt_Reg_3052(0x10,0x2B);

Wrt_Reg_3052(0xFF,0x30);
Wrt_Reg_3052(0xFF,0x52);
Wrt_Reg_3052(0xFF,0x00);
Wrt_Reg_3052(0x36,0x09);
Wrt_Reg_3052(0x11,0x00);
Delay_ms(200);
Wrt_Reg_3052(0x29,0x00);
Delay_ms(10);
```