1/7” VGA CMOS Image Sensor

GC0307 Data Sheet

V 2.0

GALAXYCORE INC.

Document Revision History

Version	Date	Content	Amendment
1.1	2008 年 11 月	文档建立	
1.2	2008 年 12 月	统一 pin 脚	
2.0	2009 年 2 月	增加图像方向指示	

Content

Chapter1. Product Introuduction

1.1 Technical Indexes Of Product

Introduction

GC0307 is a GalaxyCore's new VGA type CMOS image sensor , It has integrated the innovated pixel technology with advanced image signal processing module to provide a full functionality of a single chip VGA camera system . This product can output kinds of different size, such as VGA, manifold mode CIF、QVGA etc, and keep the same field of view , or more quicker frame rate.

User can set register to control the image's performance by 2-wire bidirectional synchronous serial bus. This sensor can output VGA-size at 30 frames per-second(fps). It also has function as AEC、AWB、LSC etc.

Function

- 4T, pixel 3.2μx 3.2 μ,
- 1/7 inch VGA
- 10bit ADC ,programmable analog gain
- Standard serial communication interface compatible with I2C interface
- Supports Raw RGB 、 YCbCr and RGB565 etc formats
- Programmable VB、HB, any size of window select， mirror and upside down
- AWB
- AEC
- ABLC
- LSC
- Defect removal and noise removal
- Edge enhance
- CC
- Gamma
- Contrast、Saturation
- HUE adjustment
- Negative、relief etc Effect

Applications

- Cell Phone
- MP4
- PC camera
- Toys
- Monitoring
- Others

Specifications

Array size	VGA	640 x 480
Pixel size		3.2μx 3.2 μ
Power supply		2.8V (±0.2V)
Power supply current		20 mA (operating)
Standby current		10μA (standby)
Output mode (8-bit)		Raw RGB YUV/YCbCr 4:2:2 RGB565/555/444
Optical format		1/7"
Chief ray angle		25°
Image transfer rate (Max)	VGA	30 fps @24 Mhz
	CIF	80 fps @ 24 Mhz
	QVGA	90 fps @24 Mhz
	QQVGA	120 fps @ 24 Mhz
S/N Ratio		～42 dB
Scan mode		Progressive
Maximum expose		4095 Row time
A/D Converter		10 bit
Packaging		CSP/PLCC/Wafer

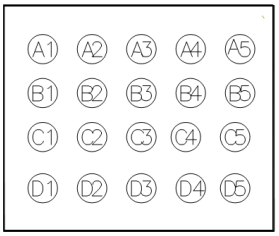


Figure 1 GC0307 Pin Diagram

(Top View)

1.2 Pin Description

Pin Number	Name	Type	Description
A1	AVDD25	Power	Analog Power，2.5V，internal generated，connect to ground via 0.1μF or 1uF capacitor
A2	VREF	Power	Reference voltage, connect to ground via 0.1μF capacitor
A3	SBDA	I/O	Serial Bus Data I/O
A4	SBCL	Input	Serial Bus Clock In
A5	D7	Output	YUV/RGB Data output bit[7]
B1	GND	Ground	Analog/Digital ground
B2	PWDN	Input	0：normal working mode 1：power down mode
B3	HSYNC	output	Horizontal sync signal output
B4	D6	output	YUV/RGB Data output bit[6]
B5	D5	output	YUV/RGB Data output bit[5]
C1	VSYNC	output	Vertical (frame) sync signal output
C2	D0	output	YUV/RGB Data output bit[0]
C3	D3	output	YUV/RGB Data output bit[3]
C4	D4	output	YUV/RGB Data output bit[4]
C5	PCLK	output	Output PCLK
D1	DVDD28	Power	Power , connect to ground via 0.1μF capacitor
D2	D1	Output	YUV/RGB Data output bit[1]
D3	D2	Output	YUV/RGB Data output bit[2]
D4	DVDD18	Power	1.8V power for digital core, internal generated, connect to ground via 0.1μF or 1uF capacitor
D5	IN_CLK	input	Master clock input

a. D[7:0] 8 bit YUV or RGB data（D[7]MSB, D[0] LSB）

b. RESETB Pin did not exiting in the package, it has been pull up to high inside chip。

1.3 GC0307 Funciton Mode

GC0307 Functions：

- Pixel Array
- Clock generator
- Analog signal processor
- A/D convertor
- Testing pattern generator
- Digital signal processor
- Window sizing
- Serial Communication Bus

Pixel Array

GC0307 image sensor has pixel array of 640x480 (307, 200 pixels).

Coclk Generator

Clock generator has following functions:

- Control pixel array and search address
- Frame rate control
- Control exposure
- Output external sync signals（VSYNC, HSYNC, and PCLK）

Analog Singal Processing

This module control analog related functions， include：

- Correlative double sampling circuit
- Signal sample/hold circuit
- Programmable Gain Amplifier circuit.

A/D Convertor

After analog signal processing，raw image data which is in Bayer pattern will be converted to 10bits digital signal.

Testing Pattern Generator

Testing Pattern Generator can produce the fixed test image for debugging and monitor calibration.

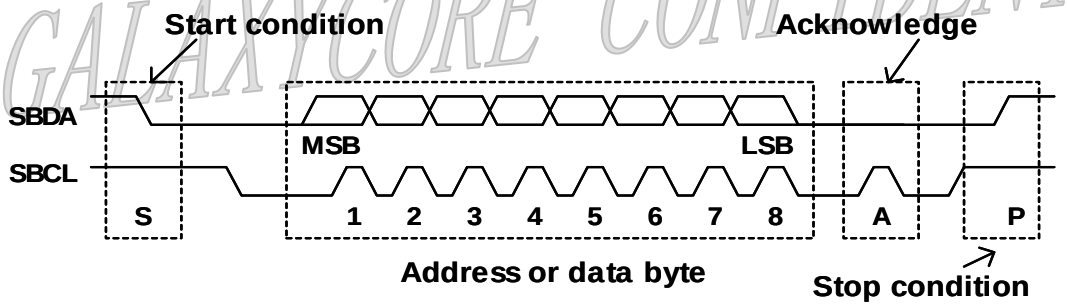
Digital Signal Processor

- Black calibration
- Lens shading compensation
- Defect removal and noise removal
- Interpolation and Edge detection
- Skin correction
- Gamma control
- YC domain processing
- Auto Situation control
- Auto expose control
- Auto White balance
- Negative、relief etc Effect

Chapter 2. Serial Bus Communication

2.1 Serial Bus Communication

GC0307uses standard serial bus I2C protocol。Serial bus writing device ID is 42H.;Serial bus reading device ID is 43H.



, .

Figure 3 Serial Communication State Diagram

S	42H	A	Register Address	A	Data	A	P

Figure 4 Command Sequence for Single Write

S	42H	A	Register Address	A	Data 1	A	…	DataN	A	P

Figure 5 Command Sequence for Incremental Writes

S	42H	A	Register Address	A	S	43H	A	DataR	NA	P

Figure 6 Command Sequence for Single Reads

S	42H	A	Register Address	A	S	43H	A	DataR1	A	…	DataRN	NA	P

Figure 7 Command Sequence for Incremental Reads

*Note:

: from master to slave

:from slave to master

S: Start

P: Stop

A: Acknowledge bit. (If there are more data to be read, send back "A")

NA: None-acknowledge bit. (If there are no more data to be read, send back "NA")

42H: Writing Address (8 bits)

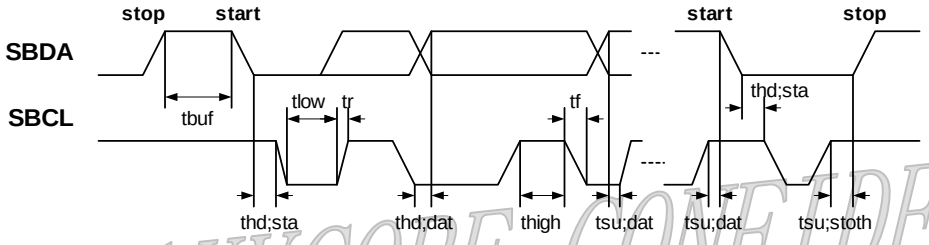
43H: Reading Address (8 bits)

Register Address: Register Address (8 bits)

Data1， …， DataN: data to be written (8 bits)

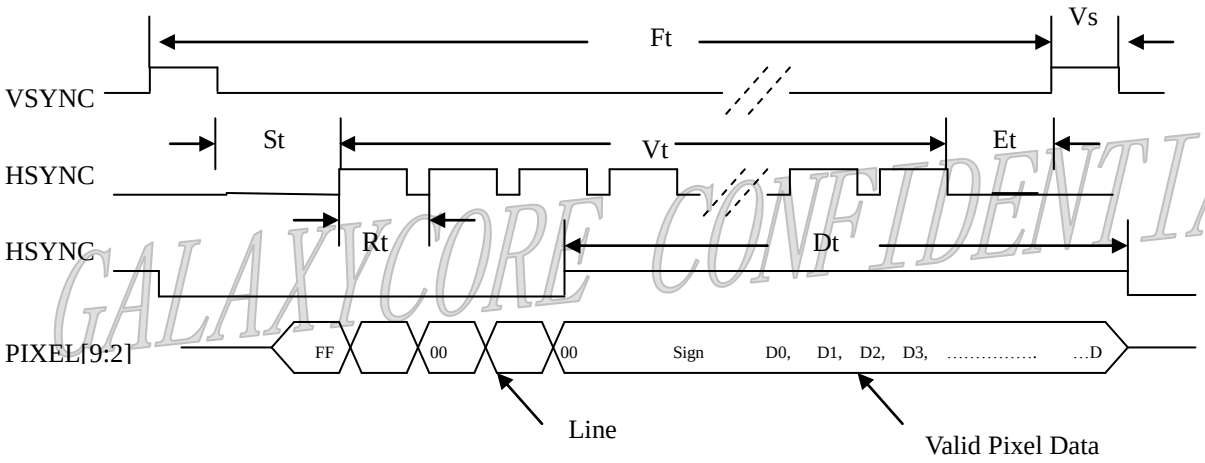
DataR1， …， DataRN: data to be read (8 bits)

2.2 Serial Bus Timing



Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	Fscl	0	400	KHz
Bus free time between a **stop** and a **start**	Tbuf	1.2	*	μs
Hold time for a repeated **start**	thd;sta	1.0	*	μs
LOW period of SBCL	Tlow	1.2	*	μs
HIGH period of SBCL	Thigh	1.0	*	μs
Set-up time for a repeated **start**	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	Tr	*	250	ns
Fall time of SBCL, SBDA	Tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

2.3 Frame Timing



Parameter	Name	EQUATION	Eg.(VGA，YUV output，@24MHz)
Rt	Frame time	Rt = window_width + 54 + HB;	window_width=640 HB=106 Rt=800*(1/12M) =10ms
Rn	Row Number	Rn = window_height+VB	window_height=488 VB=112 Rn=600
Ft	Total Frame time	Ft = Rt*Rn (exp<Rn) = Rt*exp (exp>Rn)	Ft=800*600*(1/12M) =40ms
Dt	HSYNC Width	Dt = window_width raw RGB same as YUVmode	640
St	Frame Start time	St= [reg0x1c]*Rt (Raw RGB) =[reg0x1c+8]*Rt(YUV mode)	2
Et	Frame End time	Et =[reg0x1d]* Rt	2
Vs	VSYNC High Time	Vs = (VB-St-Et)* Rt;	

*Note：set VB must meet： VB> (St+Et)

2.3 Electrical Characteristic

Symbol	Parameter	Min	Typ	Max	Unit
DVDD28	Power Supply	2.6	2.8	3.3	V
I_{DDA}	Power Supply Current		20		mA
$I_{DDS-PWDN}$	Standby Current		10	20	uA
V_{IH}	Input voltage HIGH	0.7* DVDD28			V
V_{IL}	Input voltage LOW			0.3* DVDD28	V
V_{OH}	Output voltage HIGH	0.9* DVDD28			V
V_{OL}	Output voltage LOW			0.1* DVDD28	V

Table 2 DC Characteristics

Chapter 3 . Register Related

3.1 Register

*Note: P0(page0),P1(page1)

Address	Register Name		Bits	Default	R/O	Description
P0:0x00	Chip_ID		8	0x99	RO	Chip ID ,Read only
P0:0x01	HB[7:0]		8	0x6a	RW	Horizontal blanking, unit: pixel processing time
P0:0x02	VB[7:0]		8	0x70	RW	Vertical blanking, unit: line process time. It can be used individually or combined with Hb to control frame rate. If expose time < (Vb + window Height) , frame rate will be controlled by(Vb + window Height). Otherwise frame rate will be controlled by expose time
P0:0x03	Exp	high	4	0x096	RW	Expose time，unit: line process time，0x03 for the high 4 bits of expose，0x04 for the low 8 bits of expose register
P0:0x04		low	8			
P0:0x05	Row_start	high	1	0x00	RW	Row starting
P0:0x06		low	8			
P0:0x07	Col_start	high	2	0x00	RW	COL starting
P0:0x08		low	8			
P0:0x09	Window_height	high	1	0x1e8	RW	Window height
P0:0x0a		low	8			
P0:0x0b	Window_width	high	2	0x280	RW	Window width
P0:0x0c		low	8			
P0:0x0d	rsh_width		8	0x22	RW	[7:4]restg_width [3:0]sh_width
P0:0x0e	CISCTL_mode2		8	0x02	RW	Control mode 2 [7] reserved [6] hsync mode 1: hsync always on 0: hsync only valid at active output [5] reserved [4:3] output_mode 1 0 : CIF 0 1: evenskip 0 0: VGA

					[2] reserved [1:0] exp_mode
P0:0x0f	CISCTL_mode1	8	0x32	RW	Control mode 1 [7] pad_8mA [6] reserved [5] upside down [4] mirror [3:0] reserved
P0:0x10	VB[9:8] HB [9:8]	8	0x00	RW	High bit of HB and VB [5:4] VB[9:8] [1:0] HB[9:8]
P0:0x11	Row_tail AD_ctrl1	4	0x05	RW	[7] reserved [6:4] row_tail [3:0] AD_ctrl1
P0:0x12	Analog mode 0	8	0x70	RW	reserved
P0:0x13	CISCTL_restart Analog power down	2	0x00	RW	[7]：restart new frame [6:1]: reserved [0]: analog power down_en 0: on 1 : off When power on ,Analog circuit is closed,should set this open.
P0:0x14	Reserved	8	0x00	R	Reserved
P0:0x15	Analog mode1	8	0xba	RW	Reserved
P0:0x16	Analog mode2	8	0x13	RW	Reserved
P0:0x17	AD_ctrl2	7	0x52	RW	AD_ctrl2
P0:0x18	Analog Mode 1	7	0xc0	RW	reserved
P0:0x19	PGA1	3	0x06	RW	reserved
P0:0x1a	PGA2	3	0x06	RW	reserved
P0:0x1b	reserved	8	0x00	RW	reserved
P0:0x1c	vs_st	8	0x02	RW	Frame start blank
P0:0x1d	vs_et	8	0x02	RW	Frame end blank
P0:0x1e	Tsp_width	8	0x0d	RW	reserved
P0:0x1f	Sh_delay	8	0x32	RW	reserved

3.2 ISP Related

3.2.1 General

Address	Register Name	Bits	Default	R/O	Description
P0:0x40	Blocks_enable1	8	0x7e	RW	[7] close_frame_en [6] gamma enable [5] Edge enhancement enable [4] Interpolation enable [3] Defect removal enable [2] Noise removal enable [1] Lens-shading correction enable. [0] reserved
P0:0x41	Blocks_enable2	8	0x2f	RW	[7] HP_mode [6] Inverse color output [5] ABS_en [4] YCP_as_en [3] AEC enable [2] AWB enable. [1] Skin detect enable [0] Color correction enable
P0:0x42	Debug_mode	8	0x10	RW	[7] data_delay_half_2pclk [6] extend_opclk_mode for subsample [5] allow_hsync_in_row_tail [4] reserved [3] skin map output [2] edge map (edge enhancement value) output [1] Output defect map [0] hsync_delay_half_2pclk
P0:0x43	More boundary mode o_pclk_enable bypass_mode	7	0x00	RW	[7] more_boundary_mode, [6] o_pclk output enable 1: output o_pclk 0: disable o_pclk (reset value) [5] reserved [4:0] bypass mode
P0:0x44	Output_format	8	0xe2	RW	Output mode setting: total data bus width [9:0] [7] reserved [6] output enable, reset value is 0, that is hight-z [5] averaging neighbors croma [4] output o_pclk select

					[3:0] output bus data type setting 0x00: CbYCr Y 0x01: CrYCbY 0x02: YCbYCr 0x03: YCrYCb 0x04:reserved 0x05:reserved 0x06: RGB 565 0x07: RGB x555 0x08: RGB 555x 0x09: RGB x444 0x0a: RGB 444x 0x0b: BGRG 0x0c: RGBG 0x0d: GBGR 0x0e: GRGB 0x11: only Y 0x12: only Cb 0x13: only Cr 0x14: only R 0x15: only G 0x16: only B 0x17: reserved 0x18: reserved
P0:0x45	Subsample ratio Input sequence	8	0x27	RW	[7:5] Sub-sample row ratio 1:N, N=[1～7] Should not set as 0 [4:2] Sub-sample column ratio 1:N, N=[1～7] Should not set as 0 [1:0] define type of the first pixel 0x00: grG first 0x01: R first 0x02: B first 0x03: bgG first
P0:0x46	ISP_devid	8	0x06	RO	Reserved
P0:0x47	Mode 1	8	0x20	RW	[7] test image mode 1 [6] PGA auto [5] dark_mode，should set as 0 [4] CbCr fixed en

					[3:2] dark sequence [1] allow pclk around vsync edge [0] test image mode2
P0:0x48	Mode 2	8	0xc3	RW	[7] INBF enable，should set as 1 [6] reserved [5] AEC_ exp mode [4] ISP's CIF subsample [3:2] clock divider 0 0 : 1 fractional frequency 0 1: 1/2 fractional frequency 1 0: 1/4 fractional frequency 1 1 : 1/8 fractional frequency [1] reserved [0] reserved
P0:0x49	Dither mode	8	0x00	RW	reserved
P0:0x4a	Clock gating enable	8	0x00	RW	reserved
P0:0x4b	Mode 3	8	0x00	RW	reserved
P0:0x4c	reserved	8	0x00	RW	reserved
P0:0x4e	reserved	8	0x22	RW	reserved
P0:0x4d	sync mode	8	0x23	RW	Synchronous signal output mode [7:5] reserved [4] opclk_gated_in_subsample 1: Valid pclk gated enable, If enable, only send out the valid o_pclk at sub-sample position's. 0: send out every o_pclk whenever data is valid. [3] pclk_gated_in HB, pclk gated in HBLANK 0: not gated 1: gated [2] pclk_polarity 0: invert of isp_2pclk(isp_pclk) 1: as isp_2pclk(isp_pclk) [1] hsync_polarity 0: low valid 1: high valid [0] vsync_polarity 0: low valid 1: high valid Notice: in bypass-isp mode

P0:0x4f	AWB AEC every N	5	0x01	RW	[7:6] reserved [5:4] AWB allow every 2^N frames [3] reserved [2:0] AEC allow every N frames

3.2.2 Black Calibration

Address	Register Name	Bits	Default	R/O	Description
P0:0x35	Blk_mode	8	0x58	RW	reserved
P0:0x36	Blk_limit_value	8	0x40	RW	reserved
P0:0x37	Current G1 dark value	8	0x00	RW	Current G1 pixel type dark current value
P0:0x38	Current R dark value	8	0x00	RW	Current R pixel type dark current value
P0:0x39	Current B dark value	8	0x00	RW	Current B pixel type dark current value
P0:0x3a	Current G2 dark value	8	0x00	RW	Current G2 pixel type dark current value
P0:0x3b	Global_offset	8	0x00	RW	Global offset
P0:0x3c	Manual_offset_G1	8	0x00	RW	manual offset for G1 channel
P0:0x3d	Manual_offset_R	8	0x00	RW	manual offset for R channel
P0:0x3e	Manual_offset_B	8	0x00	RW	manual offset for B channel
P0:0x3f	Manual_offset_G2	8	0x00	RW	manual offset for G2 channel
P0:0x56	Offset_ratio	8	0x77	RW	reserved
P0:0x57	Dark_current_rate	8	0x08	RW	reserved
P0:0x58	Dark_current_ratio	8	0x88	RW	reserved
P0:0x59	Offset_mode	8	0x1f	RW	reserved

3.2.3 Pre-Gain

Address	Register Name	Bits	Default	R/O	Description
P0:0x61	G1 manual gain	8	0x80	RW	manual gain for G1 channel. 0x80=1.0 times.

P0:0x63	Red manual gain	8	0x80	RW	manual gain for Red channel. 0x80=1.0 times.
P0:0x65	Blue manual gain	8	0x98	RW	manual gain for Blue channel. 0x80=1.0 times.
P0:0x67	G2 manual gain	8	0x80	RW	manual gain for G2 channel. 0x80=1.0 times.
P0:0x68	global_manual_gain	6	0x14	RW	Global manual gain for every channel. 0x10=1.0 times

3.2.4 Color Correction(CC)

Address	Register Name	Bits	Default	R/O	Description
P0:0x69	CC_matrix_11	8	0x54	RW	Parameter1 for Color correction matrix.
P0:0x6a	CC_matrix_12	8	0xff	RW	Parameter2 for Color correction matrix.
P0:0x6b	CC_matrix_13	8	0xfe	RW	Parameter3 for Color correction matrix.
P0:0x6c	CC_matrix_21	8	0xff	RW	Parameter4 for Color correction matrix.
P0:0x6d	CC_matrix_22	8	0x5f	RW	Parameter5 for Color correction matrix.
P0:0x6e	CC_matrix_23	8	0xe1	RW	Parameter6 for Color correction matrix.

3.2.5 Lens Shading compensation(LSC)

Address	Register Name	Bits	Default	R/O	Description
P0:0x70	Decrease_gain_1	6	0x14	RW	Reserved
P0:0x71	Decrease_gain_2	6	0x1c	RW	Reserved
P0:0x72	Decrease_gain_3	6	0x20	RW	Reserved
P0:0x73	Start radius	8	0x10	RW	Start position for LSC.
P0:0x74	Row center	8	0x3c	RW	Row center for LSC
P0:0x75	Column center	8	0x52	RW	Col center for LSC.

3.2.6 Defect Removal and noise removal

Address	Register Name	Bits	Default	R/O	Description
P0:0x7d	DN_mode	7	0x0f	RW	Reserved
P0:0x7e	DN_1	8	0x35	RW	Reserved
P0:0x7f	DN_2	8	0x86	RW	Reserved
P0:0x80	DN_3	6	0x0c	RO	Reserved
P0:0x81	DN_4	6	0x0c	RO	Reserved
P0:0x82	DN_5	8	0x44	RO	Reserved
P0:0x83	DD_TH1	8	0x18	RW	Reserved
P0:0x84	DD_TH2	8	0x18	RW	Reserved
P0:0x85	DD_TH3	8	0x04	RW	Reserved
P0:0x87	DN_6	8	0x32	RW	Reserved

3.2.7 Interpolation and Edge enhance

Address	Register Name	Bits	Default	R/O	Description
P0:0x5c	Auto EE_1	8	0x84	RW	Reserved
P0:0x5d	Auto EE_2	8	0x74	RW	Reserved
P0:0x5e	reserved	8	0x00	RO	Reserved
P0:0x5f	reserved	8	0x00	RO	Reserved
P0:0x88	diretion_1	5	0x06	RW	Reserved
P0:0x89	diretion_2	4	0x02	RW	Reserved
P0:0x8a	Edge1	8	0x60	RW	[7:4] edge 1 max threshold [3:0] edge 1 min threshold
P0:0x8b	Edge2	8	0x60	RW	[7:4] edge 2 max threshold [3:0] edge 2 min threshold
P0:0x8c	Edge mode	3	0x07	RW	reserved
P0:0x8d	Edge_effect	8	0xca	RO	reserved
P0:0x86	Edge2_th	8	0x02	RW	Edge 2 threshold
P0:0x8e	Edge1_th	8	0x02	RW	Edge 1 threshold
P0:0x50	INTP_LP_mode	4	0x0c	RW	reserved
P0:0x51	Ee_dec_high	6	0x20	RW	reserved
P0:0x52	EE_dec_low	6	0x08	RW	reserved
P0:0x53	Ee_high_dec_rate EE_low_dec_rate	8	0x00	RW	reserved

3.2.8 RGB Gamma correction

* Note : Controlled by auto_gamma module ， refer auto_gamma。

Address	Register Name	Bits	Default	R/O	Description
P0:0x8f	Gamma_out 0	8	0xdb	RO	Each out value of knee_i. Knee0=0
P0:0x90	Gamma_out 1	8	0xe2	RO	Knee1=8
P0:0x91	Gamma_out 2	8	0xed	RO	Knee2=16
P0:0x92	Gamma_out 3	8	0xf6	RO	Knee3=24
P0:0x93	Gamma_out 4	8	0xfd	RO	Knee4=32
P0:0x94	Gamma_out 5	8	0x04	RO	Knee5=40
P0:0x95	Gamma_out 6	8	0x0e	RO	Knee6=48
P0:0x96	Gamma_out 7	8	0x1b	RO	Knee7=64
P0:0x97	Gamma_out 8	8	0x28	RO	Knee8=80
P0:0x98	Gamma_out 9	8	0x35	RO	Knee9=96
P0:0x99	Gamma_out 10	8	0x41	RO	Knee10=112
P0:0x9a	Gamma_out 11	8	0x4e	RO	Knee11=128
P0:0x9b	Gamma_out 12	8	0x67	RO	Knee12=144
P0:0x9c	Gamma_out 13	8	0x7e	RO	Knee13 =160
P0:0x9d	Gamma_out 14	8	0x94	RO	Knee14 = 192
P0:0x9e	Gamma_out 15	8	0xa7	RO	Knee15 = 224
P0:0x9f	Gamma_out 16	8	0xba	RO	Knee16 = 256

3.2.9 Skin Correction

Address	Register Name	Bits	Default	R/O	Description
P0:0xa8	skin_Cb_center	8	0xee	RW	Parameter1 for skin detection.
P0:0xa9	skin_Cr_center	4	0x12	RW	Parameter2 for skin detection.
P0:0xaa	skin_radius_high	4	0x01	RW	Parameter3 for skin detection.
P0:0xab	skin_radius_low	8	0x20	RW	Parameter4 for skin detection.
P0:0xac	Skin B high limit	8	0xf0	RW	Parameter5 for skin detection.
P0:0xad	Skin B low limit	8	0x10	RW	Parameter6 for skin detection.

3.2.10 YC domain processing

Address	Register Name	Bits	Default	R/O	Description
P0:0xa0	Saturation	8	0x40	RW	Global saturation, controlled by auto_saturation.
P0:0xa1	luma_contrast	8	0x40	RW	Luma_contrast, notice center can be moved by 0x77. 1.7bits, 0x40=1.0
P0:0xa2	saturation_Cb	8	0x48	RW	Cb saturation S2.5bits, 0x20=1.0
P0:0xa3	saturation_Cr	8	0x48	RW	Cr saturation S2.5bits, 0x20=1.0
P0:0xa4	AS_high B start	8	0xc8	RW	High B start
P0:0xa5	AS_high B slope	8	0x02	RW	High B slope
P0:0xa6	AS_low B start	8	0x28	RW	Low B start
P0:0xa7	AS_low B slope	8	0x02	RW	Low B slope
P0:0x77	Contrast center	8	0x80	RW	Contrast center value
P0:0x78	Fixed_Cb	8	0x00	RW	When fixed_CbCr(0x47[4]) is on, Cb Cr value will be replaced by them. S7
P0:0x79	Fixed_Cr	8	0x00	RW	
P0:0x7a	Luma_offset	8	0x00	RW	Add offset on luma value. S7.

P0:0x7b	Hue_cos	8	0x40	RW	Used for hue adjustment. S1.6 Cb' = hue_cos*Cb – hue_sin*Cr Cr' = hue_sin*Cb + hue_cos*Cr
P0:0x7c	Hue_sin	8	0x00	RW	

3.2.11 ABS

Address	Register Name	Bits	Default	R/O	Description
P0:0xae	ABS_1	8	0x50	RW	Reserved
P0:0xaf	ABS_2	8	0x74	RW	Reserved
P0:0xb0	Y_black_level	8	0xe0	RO	When ABS_en(0x41[5]) is on, it is controlled by ABS module. When ABS_en is off, user can write it. S7
P0:0xb1	ABS_3	8	0x20	RW	Reserved
P0:0xb2	ABS_4	8	0x6c	RW	Reserved
P0:0xb3	ABS_5	7	0x40	RW	Reserved
P0:0xb4	ABS_6	8	0x04	RW	Reserved

3.2.12 Auto Saturation

Address	Register Name	Bits	Default	R/O	Description
P0:0xb5	Exp_low	8	0x70	RW	Auto saturation exposure low threshold
P0:0xb6	Gain_high	8	0x40	RW	Gain high threshold
P0:0xb7	Exp_slope	8	0x00	RW	Exposure slope
P0:0xb8	Gain slope	8	0x38	RW	Gain slope
P0:0xb9	Saturation limit	8	0xc3	RW	Saturation limit
P0:0xba	Total gain mode	4	0x0f	RW	Reserved

3.2.13 Auto White Balance (AWB)

Address	Register Name	Bits	Default	R/O	Description
P0:0xbb	AWB_0	8	0x42	RW	Parameter1 for AWB function.
P0:0xbc	AWB_1	8	0x60	RW	Parameter2 for AWB function.
P0:0xbd	AWB_2	8	0x50	RW	Parameter3 for AWB function.
P0:0xbe	AWB_3	8	0x50	RW	Parameter4 for AWB function.
P0:0xbf	AWB_4	8	0x0c	RW	Parameter5 for AWB function.
P0:0xc0	AWB_5	4	0x06	RW	Parameter6 for AWB function.
P0:0xc1	AWB_6	8	0x70	RW	Parameter7 for AWB function.
P0:0xc2	AWB_7	8	0xf4	RW	Parameter8 for AWB function.

P0:0xc3	AWB_8	8	0x40	RW	Parameter8 for AWB function.
P0:0xc4	AWB_9	8	0x18	RW	Parameter10 for AWB function.
P0:0xc5	AWB speed AWB margin	8	0x33	RW	[7] reserved [6:4] AWB gain adjust speed, the bigger the quicker. [3:0] AWB adjust margin
P0:0xc6	AWB_mode	8	0x1d	RW	Reserved
P0:0xc7	Current R gain	8	0x49	RO/RW	Current frame AWB gain When AWB is on, they are controlled by AWB. When AWB is off, user can write them for manually adjust.
P0:0xc8	Current G gain	8	0x40	RO/RW	
P0:0xc9	Current B gain	8	0x4a	RO/RW	
P0:0xca	R_gain_limit	8	0x70	RW	AWB gain limit in R channel.
P0:0xcb	G_gain_limit	8	0x70	RW	AWB gain limit in G channel.
P0:0xcc	B_gain_limit	8	0x78	RW	AWB gain limit in B channel.
P0:0xcd	R_ratio	8	0x80	RW	After AWB adjust color gains, user can arbitrary tune the color ratio of R/G/B. Float 1.7，0x80=1.0
P0:0xce	G_ratio	8	0x7f	RW	
P0:0xcf	B_ratio	8	0x80	RW	

3.2.14 Auto Exposure Control(AEC)

Address	Register Name	Bits	Default	R/O	Description
P0:0x20	AEC_1	8	0x02	RW	[7:4]reserved [3:2] measure window mode [1:0] center weight, weight for center window
P0:0x21	max post_gain	8	0xc0	RW	post_gain max limit
P0:0x22	max pre gain	8	0x60		pre_gain max limit
P0:0x23	AEC_ignore	8	0x88	RW	[7] ignore_mode [6:0]ignore_same_value
P0:0x24	AEC fast margin AEC_fast_speed	8	0x96	RW	[7:4] AEC fast margin, X4 [3] reserved [2:0] AEC fast speed
P0:0x25	AEC_low_range	8	0x30	RW	Low range threshold

P0:0x26	AEC_high_range	8	0xd0	RW	High range threshold
P0:0x27	reserved	8	0x00	RW	Reserved
P0:0x28	AEC_exp level_1 high	4	0x02	RO	[7:4] reserved [3:0] AEC exposure level 1 high 4 bits
P0:0x29	AEC_exp level_1 low	8	0x58	RO	AEC exposure level 1 low 8 bits this defines the fastest frame rate
0x2a	AEC_exp level_2 high	4	0x03	RO	[7:4] reserved [3:0] AEC exposure level 2 high 4 bits
P0:0x2b	AEC_exp level_2 low	8	0x84	RO	AEC exposure level 2 low 8 bits, lower frame rate
P0:0x2c	AEC_exp_ level_3 high	4	0x07	RO	[7:4] reserved [3:0] AEC exposure level 3 high 4 bits
P0:0x2d	AEC_exp_ level_3 low	8	0x08	RO	AEC exposure level 3 low 8 bits, more lower frame rate
P0:0x2e	AEC_exp_ level_4 high	4	0x0d	RO	[7:4] reserved [3:0] AEC exposure level 4 high 4 bits
P0:0x2f	AEC_exp_ level_4 low	8	0x7a	RO	AEC exposure level 4 low 8 bits, the lowest frame rate
P0:0x30	PGA_gain	8	0x20	RO	Current PGA gain indicator
P0:0x31	PGA_offse t	8	0x00	RO	PGA offset indicator
P0:0x32	PGA_code	8	0x1c	RO	PGA code for PGA controller
P0:0x33	exp change gain	8	0x90	RW	Exposure change gain ratio, float 1.7
P0:0x34	PD_ratio	8	0x10	RW	Reserved
P0:0xd0	AEC measure mode	8	0x34	RW	[7:6] AEC close frame number [5:4] skin_weight [3] skip mode [2] measure_point, 1: before gamma, 0: after gamma [1] want PGA mosde [0] delta exp mode

P0:0xd1	target_Y	8	0x55	RW	expected luminance value
P0:0xd2	allow_margin AEC_speed	7	0xf2	RW	[7:4] Luminance margin [3] reserved [2:0]AEC slow speed
P0:0xd3	Y_average	8	0x00	RO	Current frame luma average
P0:0xd4	AEC delta exp	8	0x96	RW	When delta_exp_mode open, exp will increase or decrease by this value.
P0:0xd5	AEC step2 sunlight	8	0x10	RW	When exp smaller than flicker step, it will choose this step's integer times value.
P0:0xd6	anti_flicker_step	8	0x96	RW	Exp will choose this value's integer times to avoid flicker.
P0:0xd7	exp_min_l	8	0x40	RW	Expose minimum value of low 8bit
P0:0xd8	Exp_min_l[11:8] Pga_change_times	8	0x02	RW	[7:4] high 4bit of Expose minimum value . [3:0] Pga_change_times
P0:0xd9	reserved	8	0x00	RW	reserved
P0:0xda	reserved	8	0x00	RW	reserved
P0:0xdb	Auto_post_gain	8	0x00	RO/RW	Precision float 2.6 When AEC on, it will controlled by AEC When AEC off, user can write it.
P0:0xdc	Auto_pre_gain	8	0x00	RO/RW	Precision float 2.6 When AEC on, it will controlled by AEC When AEC off, user can write it.
P0:0xdd	Max_exp_level AAA_skip_mode	8	0x22	RW	[7:6] reserved [5:4] AEC max exposure level . [3] reserved [2] reserved [1] AWB skip mode [0] ABS skin mode
P0:0xde	reserved	8	0x00	RW	reserved
P0:0xdf	reserved	8	0x00	RW	reserved

3.2.15 Measure window

*Note: AWB/AEC/ABS share one window setting

Address	Register Name	Bits	Default	R/O	Description
P0:0xe0	big_win_x0	8	0x03	RW	Measure big window left column number

P0:0xe1	big_win_y0	8	0x02	RW	Measure big window left row number
P0:0xe2	big_win_x1	8	0x27	RW	Measure big window right column number
P0:0xe3	big_win_y1	8	0x1e	RW	Measure big window right row number
P0:0xe8	Small_win_w1	8	0x3b	RW	Small window width 1
P0:0xe9	Small_win_w2	8	0x6e	RW	Small window width 2
P0:0xea	Small_win_h1	8	0x2c	RW	Small window height 1
P0:0xeb	Small_win_h2	8	0x50	RW	Small window height 2
P0:0xec	Small_win_h3	8	0x73	RW	Small window height 3
P0:0xed	Close_frame1	8	0x00	RW	Close frame number1
P0:0xee	Close_frame2	8	0x00	RW	Close frame number2
P0:0xef	Close_frame3	4	0x00	RW	[7:4] N/A [3:0]Close frame number

3.2.16 PGA Control table

*Note: When setting auto_PGA, user should configure this table.

Address	Register Name	Bits	Default	R/O	Description
P1: 0x00	PGA_gain_0	8	0x20	RW	Parameter1 for PGA control.
P1:0x01	PGA_gain_1	8	0x20	RW	Parameter2 for PGA control.
P1:0x02	PGA_gain_2	8	0x20	RW	Parameter3 for PGA control.
P1:0x03	PGA_gain_3	8	0x20	RW	Parameter4 for PGA control.
P1:0x04	PGA_gain_4	8	0x78	RW	Parameter5 for PGA control.
P1:0x05	PGA_gain_5	8	0x78	RW	Parameter6 for PGA control.
P1:0x06	PGA_gain_6	8	0x78	RW	Parameter7 for PGA control.

P1:0x07	PGA_gain_7	8	0x78	RW	Parameter8 for PGA control.
P1:0x10	PGA_gain_0_code	8	0x04	RW	Parameter9 for PGA control.
P1:0x11	PGA_gain_1_code	8	0x04	RW	Parameter10 for PGA control.
P1:0x12	PGA_gain_2_code	8	0x04	RW	Parameter11 for PGA control.
P1:0x13	PGA_gain_3_code	8	0x04	RW	Parameter12 for PGA control.
P1:0x14	PGA_gain_4_code	8	0x01	RW	Parameter13 for PGA control.
P1:0x15	PGA_gain_5_code	8	0x01	RW	Parameter14 for PGA control.
P1:0x16	PGA_gain_6_code	8	0x01	RW	Parameter15 for PGA control.
P1:0x17	PGA_gain_7_code	8	0x01	RW	Parameter16 for PGA control.
P1:0x20	PGA_offset_0	8	0x00	RW	Parameter17 for PGA control.
P1:0x21	PGA_offset_1	8	0x00	RW	Parameter18 for PGA control.
P1:0x22	PGA_offset_2	8	0x00	RW	Parameter19 for PGA control.
P1:0x23	PGA_offset_3	8	0x00	RW	Parameter20 for PGA control.
P1:0x24	PGA_offset_4	8	0x00	RW	Parameter21 for PGA control.
P1:0x25	PGA_offset_5	8	0x00	RW	Parameter22 for PGA control.
P1:0x26	PGA_offset_6	8	0x00	RW	Parameter23 for PGA control.
P1:0x27	PGA_offset_7	8	0x00	RW	Parameter24 for PGA control.
P1:0x40	PGAC mode	8	0x11	RW	Reserved.

3.2.17 PAGE1

Address	Register Name	Bits	Default	R/O	Description
LSC					
P1:0x45	LSC_red_b2	8	0x06	RW	Parameter1 for the red channel of LSC.
P1:0x46	LSC_green_b2	8	0x06	RW	Parameter1 for the green channel of LSC.
P1:0x47	LSC_blue_b2	8	0x05	RW	Parameter1 for the blue channel of LSC.
P1:0x48	LSC_red_b4	8	0x04	RW	Parameter2 for the red channel of LSC.
P1:0x49	LSC_green_b4	8	0x03	RW	Parameter2 for the green channel of LSC.
P1:0x4a	LSC_blue_b4	8	0x03	RW	Parameter2 for the blue channel of LSC.
More AWB parameters					
P1:0x62	AWB_left_Cb	8	0xd8	RW	Parameter1 for AWB left range
P1:0x63	AWB_left_Cr	8	0x24	RW	Parameter2 for AWB left range
P1:0x64	AWB_left_C_max	8	0x24	RW	Parameter3 for AWB left range
P1:0x65	AWB_right_Cb	8	0x24	RW	Parameter1 for AWB right range
P1:0x66	AWB_right_Cr	8	0xd8	RW	Parameter2 for AWB right range
P1:0x67	AWB_right_C_max	8	0x24	RW	Parameter3 for AWB right range

Additional CC matrix					
P1:0x69	CC_mode	2	0x03	RW	[7:2] N/A [1] CC_mode [0]Range_mode
P1:0x70	CC_matrix_11_G	8	0x5d	RW	Parameter1 for G range.
P1:0x71	CC_matrix_12_G	8	0xed	RW	Parameter2 for G range.
P1:0x72	CC_matrix_13_G	8	0xff	RW	Parameter3 for G range.
P1:0x73	CC_matrix_21_G	8	0xe5	RW	Parameter4 for G range.
P1:0x74	CC_matrix_22_G	8	0x5f	RW	Parameter5 for G range.
P1:0x75	CC_matrix_23_G	8	0xe6	RW	Parameter6 for G range.
P1:0x76	CC_matrix_11_B	8	0x41	RW	Parameter1 for B range.
P1:0x77	CC_matrix_12_B	8	0xef	RW	Parameter2 for B range.
P1:0x78	CC_matrix_13_B	8	0xff	RW	Parameter3 for B range.
P1:0x79	CC_matrix_21_B	8	0xff	RW	Parameter4 for B range.
P1:0x7A	CC_matrix_22_B	8	0x5f	RW	Parameter5 for B range.
P1:0x7B	CC_matrix_23_B	8	0xfa	RW	Parameter6 for B range.