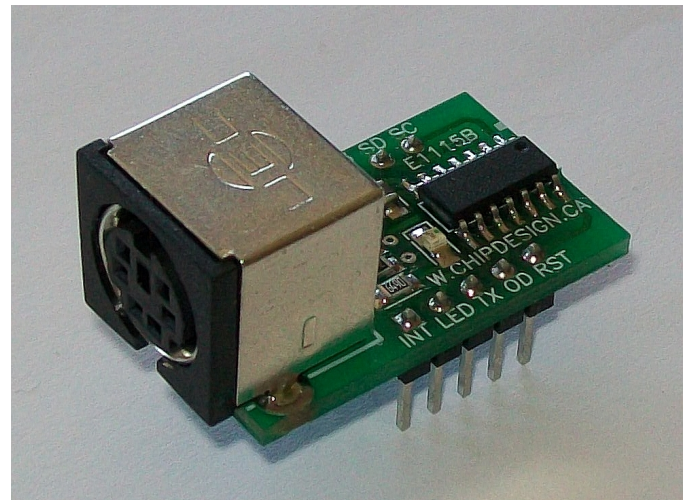


## FEATURES

- Decodes PS/2 Scanset 2 keystrokes to a single ASCII byte on make
- Offload process intensive PS/2 keyboard decoding
- Unique single byte codes for non-ASCII keys including multi-media keys
- Simple interface between PS/2 keyboard and host microcontroller
- Compatible with any microcontroller
- 115.2 Kbaud serial data output
- 100 KHz clocked serial data output
- Selectable baud rate 115.2K/56.2K
- Interrupt output
- LED flash output
- Low cost solution

## APPLICATIONS

- Enhance microcontroller applications with keyboard data
- Process control
- Robotics control



## DESCRIPTION

The E1115B PS/2 Keyboard to ASCII Converter module allows a microcontroller application to be enhanced with keyboard numeric and text data without having to handle the tedious scancode detection and decoding process. This module receives the complex scancode sequence for each keystroke on the "make", and decodes it to a unique ASCII byte which is easier to use by a host application. This frees up the host microcontroller considerably since it does not have to wait for each bit to be determined, then for each scancode byte to be saved, and finally for the variable length byte sequence to be decoded. Decoding the randomly occurring keyboard scancodes normally requires an interrupt for each keyboard clock edge, so a

host microcontroller could be interrupted up to 40 times over a several millisecond period for each keystroke. As the E1115B module is dedicated to the task and provides a single decoded byte corresponding to the keystroke, the host can concentrate on its own application while being interrupted only when necessary. Non-ASCII keys are also decoded to a unique code. The E1115B module only requires +5.0V and a connection to the host. The outputs are compatible with 3.3V and 5.0V TTL-compatible inputs. The E1115B module provides both serial data at 115.2K/57.6K and clocked serial data at ~100 KHz. An interrupt signal and a LED flash output are also provided. The E1115B module is available in a 10 pin DIP package with integrated PS/2 connector.

**Table 1. Absolute Maximum Ratings**

Parameter	Rating
V <sub>dd</sub> to GND	-0.3 to +13V
Digital input voltage to GND	-0.3 to +5.8V
Digital output voltage to GND	-0.3 to +5.8V
Operating temperature range	-40 to +85°C
Storage temperature range	-65 to +150°C
Maximum output current through port pin	100mA
Maximum total current through V <sub>dd</sub> and GND pins	500mA

**Table 2. Electrical Characteristics**

Test Conditions: Supply Voltage V<sub>dd</sub> = +5.0V, T<sub>ambient</sub> = 25° C, unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>dd</sub>	Supply voltage	4.75	5.0	5.25	V
I <sub>dd</sub>	Supply current, no keyboard		6.6		mA
V <sub>IH</sub>	Digital high input voltage	2.0			V
V <sub>IL</sub>	Digital low input voltage			0.8	V
V <sub>OH</sub>	Digital high output voltage	V <sub>dd</sub> -0.7			V
V <sub>OL</sub>	Digital low output voltage			0.6	V
T <sub>operate</sub>	Operating temperature	-40		+85	°C
T <sub>response</sub>	Response time			5	µsec
	Output baud rate	57.6		115.2	KBaud
	Output clocked data rate		~100		Kbps

**General Precautions**

Charged devices and circuit boards can discharge without warning. Proper ESD precautions should be followed to avoid failure.

This device is not authorized for use in any product where the failure or malfunction of the product can reasonably be expected to cause failure in a life support system or to significantly affect its operation.

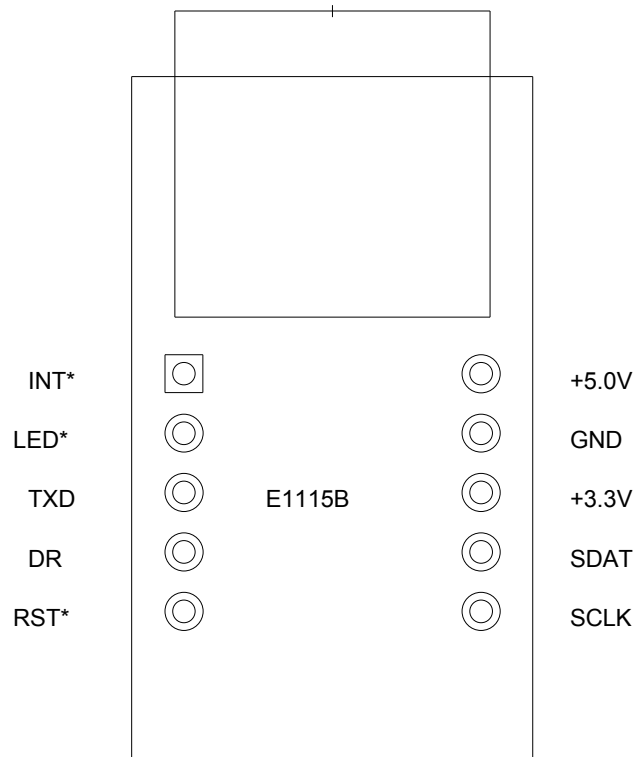
Locus Engineering Inc. reserves the right to make changes at any time without notice to improve product features or reliability.

Information is provided by Locus Engineering Inc. with the best of intentions without any warranty expressed or implied. As such Locus Engineering Inc. disclaims all liabilities or responsibilities for any use of the information, any inaccuracies or fitness for a particular purpose.

Locus Engineering Inc. (formerly CHiPdesign) as of October 2014.

**Table 3. Pin Descriptions**

Pin#	Name	Function
1	INT*	Interrupt output, 10 usec active low before and after SDAT
2	LED*	LED flash output, 8msec active low
3	TXD	115.2 K or 57.6K Baud serial data output
4	DR	Data rate select, H=115.2Kbaud, L=57.6Kbaud
5	RST*	Reset, active low input
6	SCLK	Serial clock output
7	SDAT	Clocked serial data output, ~100KHz
8	+3.3V	+3.3V regulator output, 40mA maximum
9	GND	Ground
10	+5.0V	+5.0V input to +3.3V regulator input and to PS/2 keyboard connector



**Figure 1. Pinout Diagram**

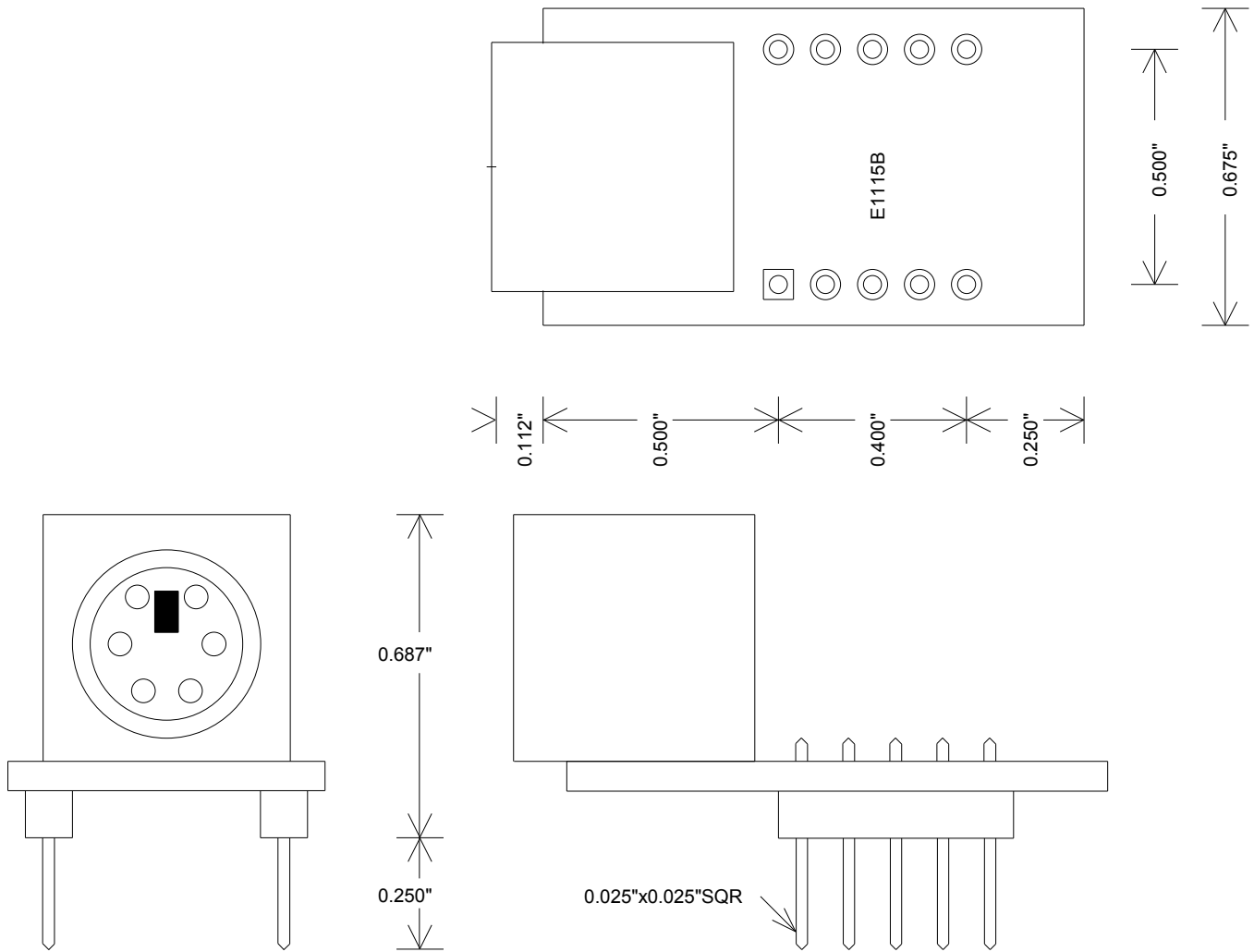
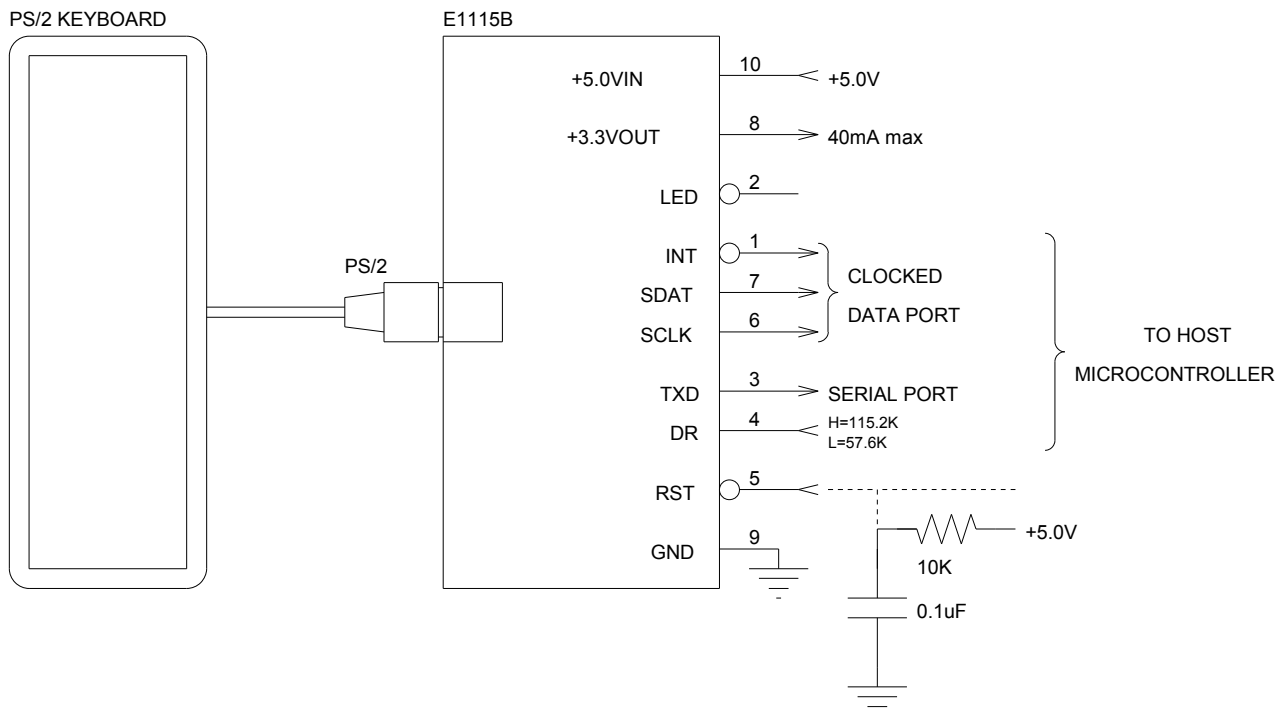


Figure 2. Module PCB Dimensions



**Figure 3. General Application Circuit**

### Power Supply

The E1115B module requires +5.0V to operate the module and power the PS/2 keyboard. The keyboard should not be connected or disconnected with the power on. The module consumes approximately 10 mA. Note that PS/2 keyboards can consume up to 200mA and that the keyboard should not be connected or disconnected with the power on.

### Reset

The power-on reset circuitry is self-contained within the chip. A reset pin is provided however it is not needed unless the power supply ramp is slower than 1msec. The optional reset source can be from a microcontroller pin or an RC combination. Typical RC values are 10K and 0.1uF respectively.

### Serial Data Port

Data is available at the serial port and at the clocked data port. The serial port is a single line connection to the host microcontroller's RXD pin. The serial data rate is selectable between 115.2K or 57.6K baud using the DR pin. Leaving the DR pin open defaults to the 115.2K baud data rate while grounding the DR pin results in the 57.6K baud data rate.

### Clocked Data Port

The clocked data port is a three line connection to the host microcontroller which includes an interrupt pulse, serial data, and an active low ~100KHz clock pulse train. A single byte is sent to the serial port and then to the clocked data port on the "make" of every keystroke. A serial to parallel shift register can be used to capture the clocked data from the E1115B. The INT\* signal can also be used to indicate that the data has finished being loaded into the shift register.

Each clocked serial data bit time is approximately 10 usec. The data is output with the most significant bit first and the output is inverted. Note that either the rising or the falling edge of the SCLK can be used to clock the SDAT into a shift register as the SCLK edges are 3.3 usec inside the bit period.

### **Interrupt Output**

The INT\* output is asserted 10  $\mu$ sec in advance and held low until 10  $\mu$ sec after the clocked serial data has been sent. This allows a host time to setup and receive the serial clock and data.

### **LED Flash Output**

An onboard LED flashes for 8 msec following the termination of the interrupt signal.

### **Module Operation**

On power up or external reset, the E1115B initializes the keyboard which flashes the CapsLock, NumLock, and ScrollLock indicators. Following the initialization, the E1115B waits for keyboard scancodes. The E1115B parses the keyboard scancodes as they are received so that the corresponding ASCII code is produced as quickly as possible. Typical response times are within 5 microseconds after the last bit of the last scancode for a keystroke is received. Note that ASCII codes are produced only on the make, i.e. when the key is pressed. No ASCII codes are produced on the release of the key.

The E1115B decodes the unshifted and shifted keys using the state of the Shift key or CapsLock key. Other control keys such as Alt, Ctrl, NumLock, and ScrollLock have no effect on the keys although outputs are produced. The CapsLock, NumLock, and ScrollLock toggle their respective indicators on the keyboard. While the CapsLock key produces no output, the NumLock and ScrollLock keys produce outputs which toggle between two values. All the non-ASCII keys on the PS/2 keyboard also produce unique codes. The E1115B allows typematic functionality where ASCII codes are repeated at a 10Hz rate when a key is held down for more than a second. The only exception to the typematic functionality is the Pause/Break key which only puts out one code when the key is held down.

The E1115B first sends data through the serial port at the selected data rate using one start bit, 8 data bits, no parity, and one stop bit (8N1 format). The INT\* line is then brought low and 10  $\mu$ sec later, the clocked data is sent. The INT\* line is held low until 10  $\mu$ sec after the end of the clocked data transmission.

Once the INT\* line is deasserted, the LED\* line is pulsed low for 8 msec. The keyboard is inhibited until all outputs are completed.

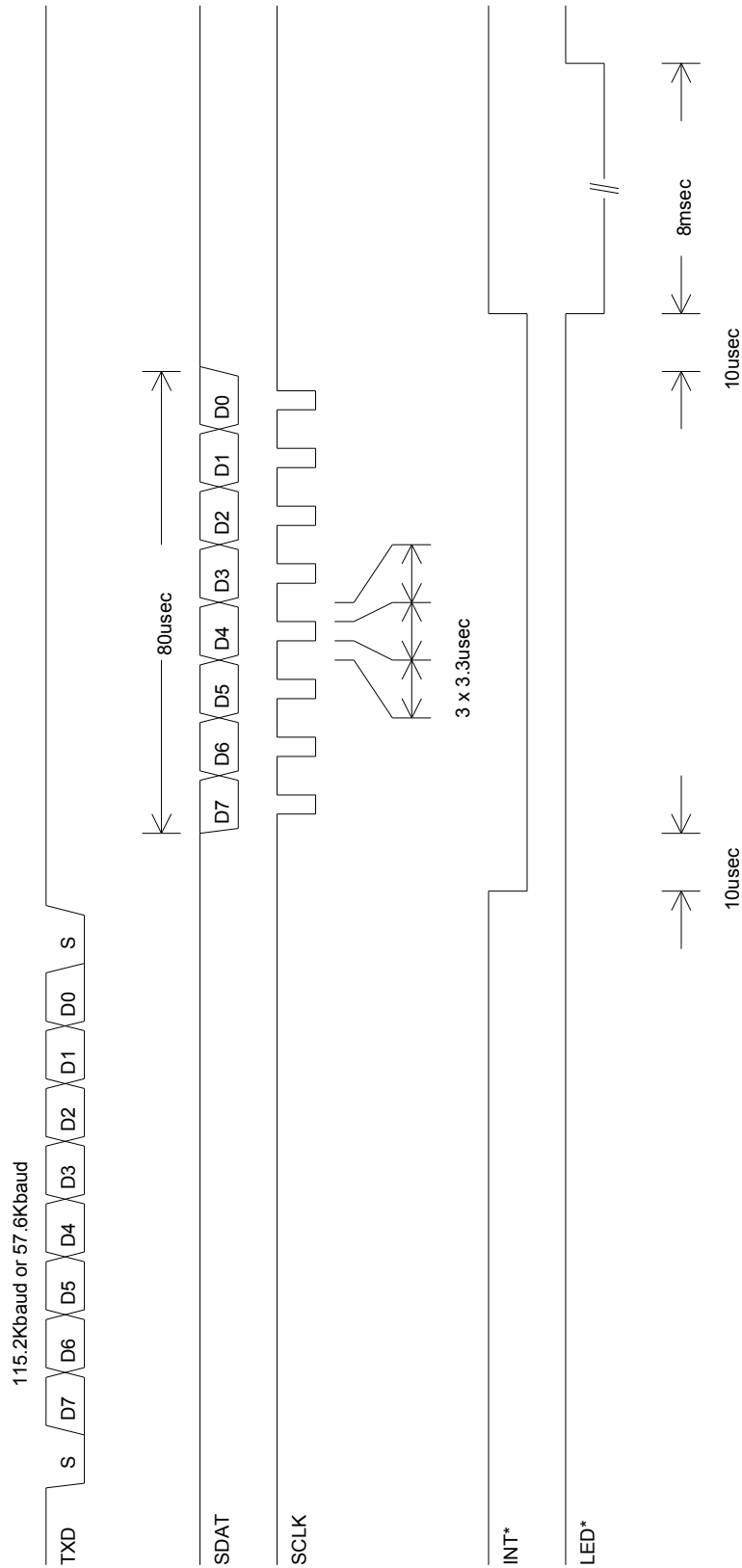
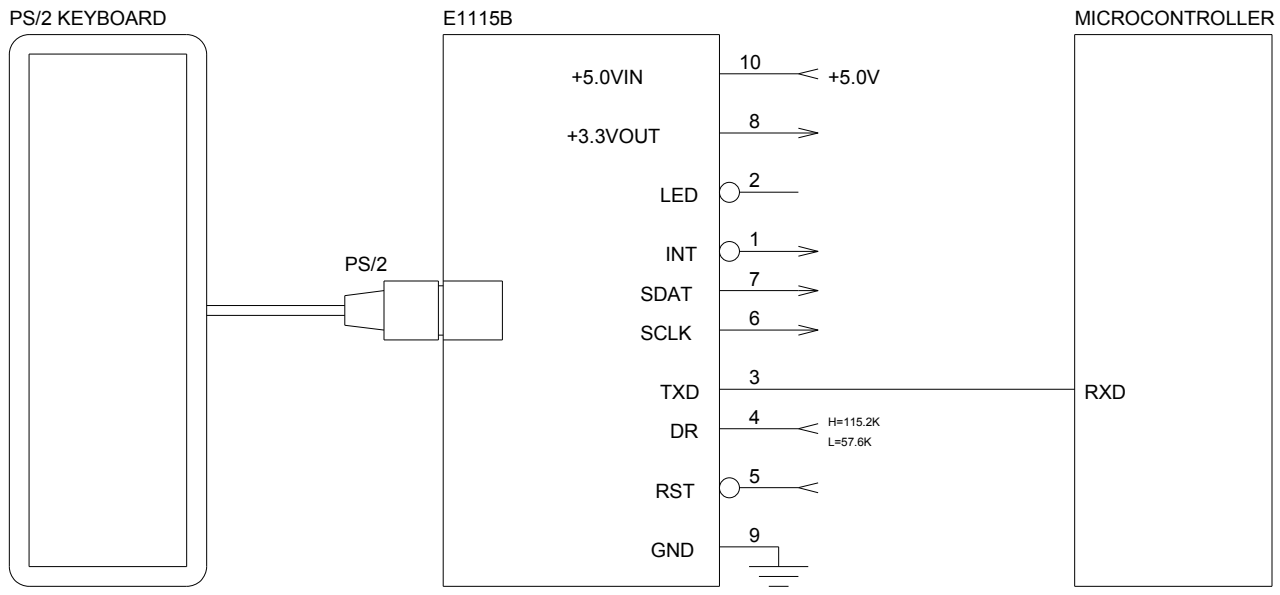


Figure 4. Signal Data Timing

## SERIAL DATA INTERFACE

The simplest protocol is a serial data transfer using the host's UART in which case only TXD is used. A typical interface to a microcontroller is shown below.



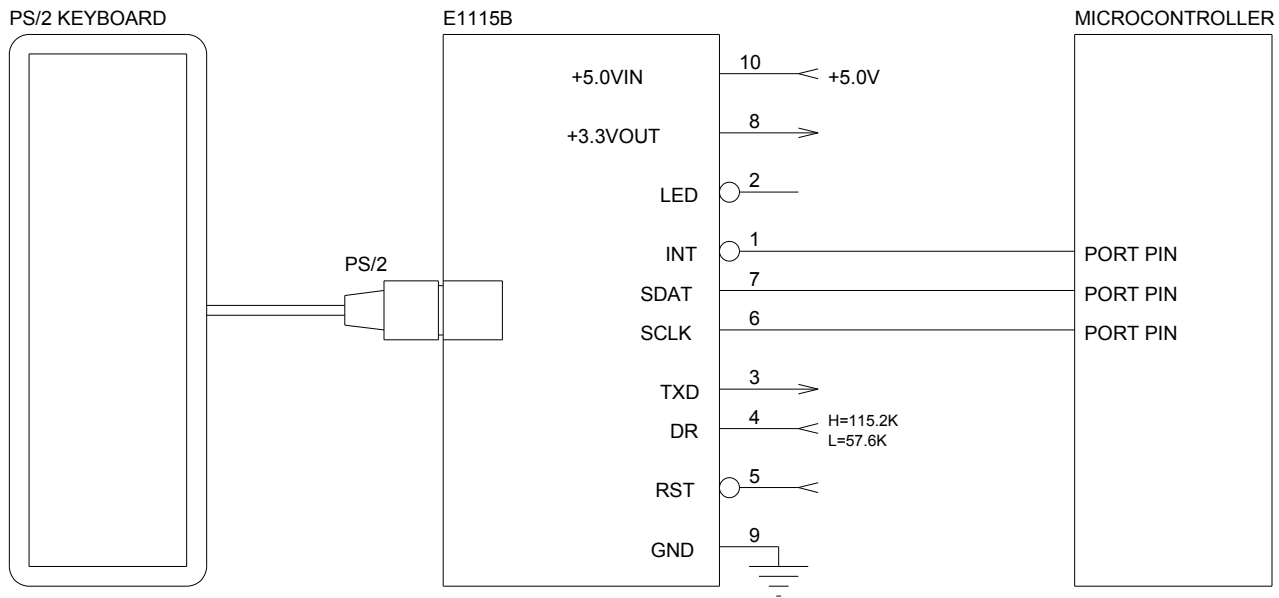
**Figure 5. Serial Interface to Microcontroller**

Data is output with the most significant bit first. The baud rate is selectable between 115.2K baud or 57.6K baud using the data rate selection pin DR. The serial data can be converted to bipolar RS-232 levels using a MAX232 type chip or equivalent.



**CLOCKED SERIAL DATA INTERFACE TO MICROCONTROLLER**

If a UART is not available on the microcontroller, data can be received using the serial data, serial clock, and INT\* signals. The INT\* signal can be used as an interrupt to the microcontroller whose falling edge occurs 10 usec prior to the first data bit. This delay allows the microcontroller to save any work in progress before reading the E1115B data. The microcontroller can read the serial data whenever the serial clock level is low, or use either clock edge to read the serial data bits which are sent most-significant-bit first.



**Figure 6. Clocked Data Interface to Microcontroller**

## CLOCKED SERIAL DATA INTERFACE TO SHIFT REGISTER

A shift register can also be used to capture the ASCII byte from the clocked serial data port. The following circuit illustrates the clocked data capture using a 74LV164 shift register. The 'LV series has TTL compatible inputs and rail to rail outputs while operating between 2.0V and 6.0V, so compatibility is maintained regardless of the shift registers' supply voltage.

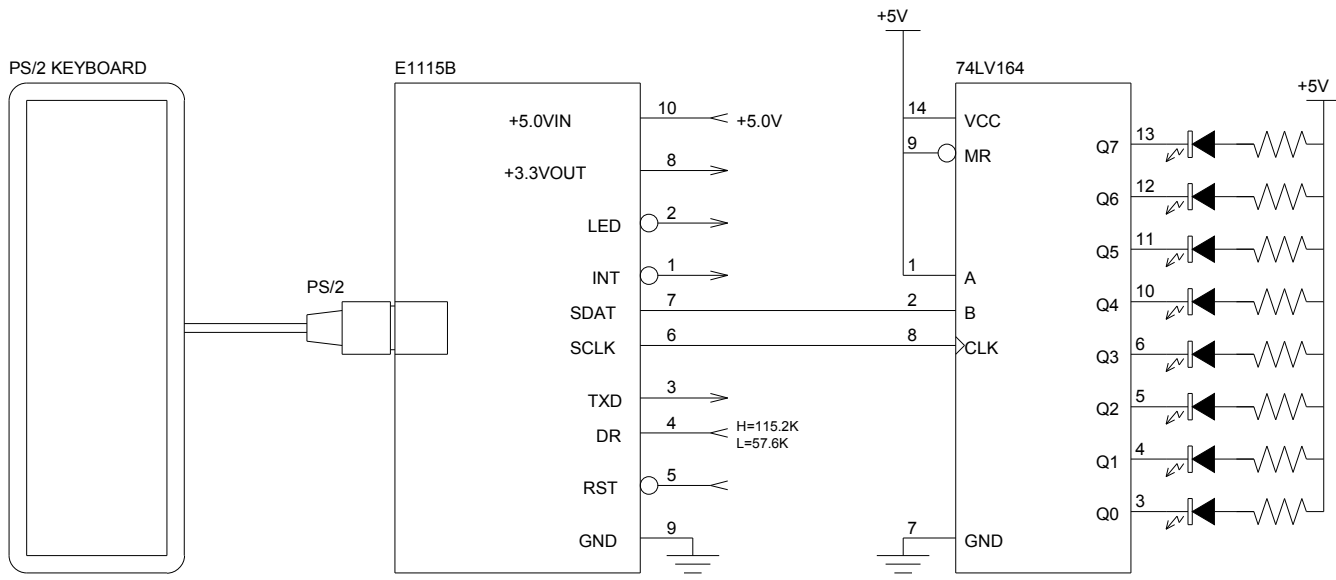


Figure 7. Clocked Data Interface to Shift Register

## KEYBOARD CODE CORRESPONDENCES

The E1115B produces ASCII codes for all standard ASCII keys and unique single byte codes for the non-ASCII keys as shown in the following tables. It should be noted that there are variations between keyboard manufacturers for the scancodes produced, especially for the multi-media keys so care is needed in selecting the same keyboard for a particular application. The output produced by the E1115B represent the most common codes from keyboards. Where there are differences between keyboard models, the codes remain unique for the same model of keyboard keys.

On the main keyboard, the CAPSLock and SHIFT keys only modify keys with upper and lower case characters. The CAPSLock key also toggles its LED. The CTRL, GUI, ALT, and APP each produce unique non-ASCII codes. Figure 11 indicates the code correspondences for the various keys.

The extended keypad code correspondences are indicated in Figure 12. Note that the SCRLock and NUMLock codes toggle between two values depending on the the state of the associated LED. Apart from the keypad arithmetic operators which have codes identical to the keys on the main keyboard, all other keys have unique non-ASCII codes.

The multi-media keypad code correspondences are all unique non-ASCII codes.



PRNT FD	SCRL 84/85	PBRK FE	NUM 82/83	/ 2F	* 2A	- 2D
INS C0	HOME C1	PGUP C2	7 D7	8 D8	9 D9	+ 2B
DEL C3	END C4	PGDN C5	4 D4	5 D5	6 D6	
	↑ DA		1 D1	2 D2	3 D3	ENT 0D
← DB	↓ DC	→ DD	0 D0	· DE		

Figure 9. Extended Keyboard Code Correspondences

POWER 9F	SLEEP A3	WAKE AF	MY COMPUTER A4	CALCULATOR 95
MEDIA SELECT AB	NEXT TRACK AA	PREVIOUS TRACK D0	STOP A2	PLAY/ PAUSE 9E
MUTE D0	VOLUME UP D0	VOLUME DOWN D0	EMAIL A8	WWW HOME A1
WWW FAVORITES 8A	WWW SEARCH 86	WWW BACK A0	WWW FORWARD 9A	WWW STOP 94
WWW REFRESH 8F				

Figure 10. Multi-Media Keyboard Code Correspondences