The TPIC6B595 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When SRCLR is low, the input shift register is cleared. When output enable (G) is held high, all data in the output buffers is held low and all drain outputs are off. When G is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C = 25^\circ C$. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B595 is characterized for operation over the operating case temperature range of $-40^\circ C$ to $125^\circ C$. 
logic diagram (positive logic)
schematic of inputs and outputs

---

**EQUIVALENT OF EACH INPUT**

**VCC**

**INPUT**

25 V

**GND**

---

**TYPICAL OF ALL DRAIN OUTPUTS**

**DRAIN**

50 V

---

20 V

**GND**

---

**absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)**

Logic supply voltage, \( V_{CC} \) (see Note 1) . 7 V

Logic input voltage range, \( V_I \) . –0.3 V to 7 V

Power DMOS drain-to-source voltage, \( V_{DS} \) (see Note 2) . 50 V

Continuous source-to-drain diode anode current . 500 mA

Pulsed source-to-drain diode anode current (see Note 3) . 1 A

Pulsed drain current, each output, all outputs on, \( I_D, T_C = 25^\circ C \) (see Note 3) . 500 mA

Continuous drain current, each output, all outputs on, \( I_D, T_C = 25^\circ C \) . 150 mA

Peak drain current single output, \( I_{DM}, T_C = 25^\circ C \) (see Note 3) . 500 mA

Single-pulse avalanche energy, \( E_{AS} \) (see Figure 4) . 30 mJ

Avalanche current, \( I_{AS} \) (see Note 4) . 500 mA

Continuous total dissipation . See Dissipation Rating Table

Operating virtual junction temperature range, \( T_J \) . –40°C to 150°C

Operating case temperature range, \( T_C \) . –40°C to 125°C

Storage temperature range . –65°C to 150°C

Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:

1. All voltage values are with respect to GND.

2. Each power DMOS source is internally connected to GND.

3. Pulse duration \( \leq 100 \mu s \) and duty cycle \( \leq 2\% \).

4. DRAIN supply voltage = 15 V, starting junction temperature (\( T_{JS} \)) = 25°C, \( L = 200 \text{ mH} \), \( I_{AS} = 0.5 \text{ A} \) (see Figure 4).

---

**DISSIPATION RATING TABLE**

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>( T_C \leq 25^\circ C ) POWER RATING</th>
<th>( T_C = 25^\circ C ) DERATING FACTOR</th>
<th>( T_C = 125^\circ C ) POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>DW</td>
<td>1389 mW</td>
<td>11.1 mW/°C</td>
<td>278 mW</td>
</tr>
<tr>
<td>N</td>
<td>1050 mW</td>
<td>10.5 mW/°C</td>
<td>263 mW</td>
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</table>
### recommended operating conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic supply voltage, $V_{CC}$</td>
<td>4.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>High-level input voltage, $V_{IH}$</td>
<td>0.85 $V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Low-level input voltage, $V_{IL}$</td>
<td>0.15 $V_{CC}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Pulsed drain output current, $T_{C} = 25^\circ C, V_{CC} = 5$ V (see Notes 3 and 5)</td>
<td>$-500$</td>
<td>$500$</td>
<td>mA</td>
</tr>
<tr>
<td>Setup time, SER IN high before SRCK↑, $t_{SU}$ (see Figure 2)</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Hold time, SER IN high after SRCK↑, $t_{H}$ (see Figure 2)</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Pulse duration, $t_{W}$ (see Figure 2)</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Operating case temperature, $T_{C}$</td>
<td>$-40$</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

### electrical characteristics, $V_{CC} = 5$ V, $T_{C} = 25^\circ C$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)DSX}$</td>
<td>Drain-to-source breakdown voltage</td>
<td>$I_D = 1$ mA</td>
<td>50</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{SD}$</td>
<td>Source-to-drain diode forward voltage</td>
<td>$I_F = 100$ mA</td>
<td>0.85</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage, SER OUT</td>
<td>$I_{OH} = -20$ µA, $V_{CC} = 4.5$ V</td>
<td>4.4</td>
<td>4.49</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OH} = -4$ mA, $V_{CC} = 4.5$ V</td>
<td>4</td>
<td>4.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage, SER OUT</td>
<td>$I_{OL} = 20$ µA, $V_{CC} = 4.5$ V</td>
<td>0.005</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{OL} = 4$ mA, $V_{CC} = 4.5$ V</td>
<td>0.3</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>High-level input current</td>
<td>$V_{CC} = 5.5$ V, $V_I = V_{CC}$</td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Low-level input current</td>
<td>$V_{CC} = 5.5$ V, $V_I = 0$</td>
<td>$-1$</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Logic supply current</td>
<td>$V_{CC} = 5.5$ V</td>
<td>All outputs off</td>
<td>20</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All outputs on</td>
<td>150</td>
<td>300</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CC(FRQ)}$</td>
<td>Logic supply current at frequency</td>
<td>$f_{SRCK} = 5$ MHz, $C_L = 30$ pF, All outputs off,</td>
<td>See Figures 2 and 6</td>
<td>0.4</td>
<td>5</td>
</tr>
<tr>
<td>$I_N$</td>
<td>Nominal current</td>
<td>$V_{DS(on)} = 0.5$ V, $N = I_D$, $T_C = 85^\circ C$</td>
<td>See Notes 5, 6, and 7</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>$I_{DSX}$</td>
<td>Off-state drain current</td>
<td>$V_{DS} = 40$ V, $V_{CC} = 5.5$ V</td>
<td>0.1</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 40$ V, $V_{CC} = 5.5$ V, $T_C = 125^\circ C$</td>
<td>0.15</td>
<td>8</td>
<td>µA</td>
</tr>
<tr>
<td>$r_{DS(on)}$</td>
<td>Static drain-source on-state resistance</td>
<td>$I_D = 100$ mA, $V_{CC} = 4.5$ V</td>
<td>4.2</td>
<td>5.7</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 100$ mA, $V_{CC} = 4.5$ V, $T_C = 125^\circ C$</td>
<td>6.8</td>
<td>9.5</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 350$ mA, $V_{CC} = 4.5$ V</td>
<td>5.5</td>
<td>8</td>
<td>Ω</td>
</tr>
</tbody>
</table>

NOTES:
3. Pulse duration $\leq 100$ µs and duty cycle $\leq 2\%$.
5. Technique should limit $T_J - T_C$ to $10^\circ C$ maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^\circ C$. 
switching characteristics, \( V_{CC} = 5 \, V \), \( T_C = 25^\circ C \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PLH} )</td>
<td>Propagation delay time, low-to-high-level output from ( \bar{G} ) ( C_L = 30 , \mu F ), ( I_D = 100 , mA ), See Figures 1, 2, and 9</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PHL} )</td>
<td>Propagation delay time, high-to-low-level output from ( \bar{G} ) ( C_L = 30 , \mu F ), ( I_D = 100 , mA ), See Figures 1, 2, and 9</td>
<td>90</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_r )</td>
<td>Rise time, drain output</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_f )</td>
<td>Fall time, drain output</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{rr} )</td>
<td>Reverse-recovery-current rise time ( I_F = 100 , mA ), ( di/dt = 20 , A/\mu s ), See Notes 5 and 6 and Figure 3</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{rr} )</td>
<td>Reverse-recovery time</td>
<td>300</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES: 5. Technique should limit \( T_J - T_C \) to \( 10^\circ C \) maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal resistance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\theta JA} )</td>
<td>Thermal resistance, junction-to-ambient ( DW ) package</td>
<td>90</td>
<td>95</td>
<td>(^\circ )C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal resistance, junction-to-ambient ( N ) package</td>
<td>All 8 outputs with equal power</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PARAMETER MEASUREMENT INFORMATION

![Test Circuit Diagram](image)

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The word generator has the following characteristics: \( t_r \leq 10 \, ns \), \( t_f \leq 10 \, ns \), \( t_w = 300 \, ns \), pulsed repetition rate (PRR) = 5 kHz, \( Z_O = 50 \, \Omega \).
B. \( C_L \) includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms
PARAMETER MEASUREMENT INFORMATION

NOTES:  
A. The word generator has the following characteristics: \( t_r \leq 10 \text{ ns} \), \( t_f \leq 10 \text{ ns} \), \( t_w = 300 \text{ ns} \), pulsed repetition rate (PRR) = 5 kHz, \( Z_0 = 50 \Omega \).
B. \( C_L \) includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode
PARAMETER MEASUREMENT INFORMATION

SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

NOTES:
A. The word generator has the following characteristics: \( t_r \leq 10 \text{ ns}, t_f \leq 10 \text{ ns}, Z_O = 50 \Omega \).
B. Input pulse duration, \( t_w \), is increased until peak current \( I_{AS} = 0.5 \text{ A} \).

Energy test level is defined as \( E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30 \text{ mJ} \).

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT

\[ I_{AS} \text{ – Peak Avalanche Current – A} \]

TIME DURATION OF AVALANCHE

\[ t_{av} \text{ – Time Duration of Avalanche – ms} \]

Figure 5

SUPPLY CURRENT

\[ I_{CC} \text{ – Supply Current – mA} \]

FREQUENCY

\[ f \text{ – Frequency – MHz} \]

Figure 6
TYPICAL CHARACTERISTICS

DRAIN-TO-SOURCE ON-STATE RESISTANCE

DRAIN CURRENT

VCC = 5 V
See Note A

TC = 125°C

TC = 25°C

TC = -40°C

Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

LOGIC SUPPLY VOLTAGE

ID = 100 mA
See Note A

TC = 125°C

TC = 25°C

TC = -40°C

Figure 8

SWITCHING TIME

CASE TEMPERATURE

ID = 100 mA
See Note A

tP

tF

tPLH

tPHL

Figure 9

NOTE C: Technique should limit TJ – TC to 10°C maximum.
THERMAL INFORMATION

**Figure 10**

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT

vs

NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

![Graph showing maximum continuous drain current versus number of outputs conducting simultaneously.](image)

- $V_{CC} = 5\, V$
- $T_C = 25^\circ C$
- $T_C = 100^\circ C$
- $T_C = 125^\circ C$

**Figure 11**

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT

vs

NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

![Graph showing maximum peak drain current versus number of outputs conducting simultaneously.](image)

- $V_{CC} = 5\, V$
- $T_C = 25^\circ C$
- $d = 10\%$
- $d = 20\%$
- $d = 50\%$
- $d = 80\%$

**Revision History**

<table>
<thead>
<tr>
<th>DATE</th>
<th>REV</th>
<th>PAGE</th>
<th>SECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>5/18/05</td>
<td>A</td>
<td>5</td>
<td>Figure 1</td>
<td>Changed SRCLR timing diagram</td>
</tr>
<tr>
<td>7/1995</td>
<td>*</td>
<td></td>
<td></td>
<td>Original reversion</td>
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**NOTE:** Page numbers for previous revisions may differ from page numbers in the current version.
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/ Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Samples (Requires Login)</th>
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</thead>
<tbody>
<tr>
<td>TPIC6B595DW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<td>TPIC6B595DWG4</td>
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<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<tr>
<td>TPIC6B595DWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<tr>
<td>TPIC6B595DWRG4</td>
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<td>DW</td>
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<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
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<tr>
<td>TPIC6B595N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>20</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- ** OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

### TAPE DIMENSIONS

![Reel Dimensions Diagram](image)

- **K0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **A0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W  (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
<tr>
<td>TPIC6B595DWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>10.8</td>
<td>13.1</td>
<td>2.65</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
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</table>

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<tbody>
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<td>SOIC</td>
<td>DW</td>
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<td>2000</td>
<td>346.0</td>
<td>346.0</td>
<td>41.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MS–013 variation AC.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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