

# HL1606

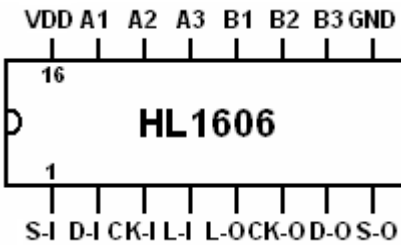
## DESCRIPTION

HL1606 is a LED driver IC with SPI controlled. We can get “complex mode changes” by fewer data.

## FEATURES

- NMOS output
- SPI controlled, plus synchronization speed control port: S-I
- PWM output, frequency: 500Hz
- With an internal “change model” unit, only data calls, reducing the amount of data.
- Speed control bit, can speed up “changes in a pixel” rate of 2 times.
- Latch enable bit, concatenated string at a point can be read or not read data.
- Built-in 6 roads, drive two pixels (three-output get a pixel)

## Pin definition



| No. | Name | Description                | No.   | Name            | Description                      |
|-----|------|----------------------------|-------|-----------------|----------------------------------|
| 1   | S-I  | Sync / speed clock input   | 7     | D-O             | Data buffer output               |
| 2   | D-I  | Data input                 | 8     | S-O             | Sync / speed clock buffer output |
| 3   | CK-I | Clock input                | 9     | GND             | GND                              |
| 4   | L-I  | Latch signal input         | 10~12 | B3~B1           | 3 way drive output               |
| 5   | L-O  | Latch signal buffer output | 13~15 | A3~A1           | 3 way drive output               |
| 6   | CK-O | Clock buffer output        | 16    | V <sub>DD</sub> | VDD                              |

## Data format

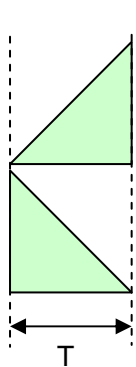
|                          |    |    |    |    |    |    |    |                          |     |     |     |     |     |     |     |        |
|--------------------------|----|----|----|----|----|----|----|--------------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| D1                       | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9                       | D10 | D11 | D12 | D13 | D14 | D15 | D16 | HIGH → |
| A1~A3 LED Control data-1 |    |    |    |    |    |    |    | B1~B3 LED Control data-2 |     |     |     |     |     |     |     |        |

Data format of A1-A3 LED Control data-1 (B1-B3 LED Control data-2 can refer it)

|                     |          |                     |          |                     |          |                      |                  |
|---------------------|----------|---------------------|----------|---------------------|----------|----------------------|------------------|
| D1 (D9)             | D2 (D10) | D3 (D11)            | D4 (D12) | D5 (D13)            | D6 (D14) | D7 (D15)             | D8 (D16)         |
| A1 (B1) Control bit |          | A2 (B2) Control bit |          | A3 (B3) Control bit |          | Control bit of speed | Latch enable bit |

|                        |                        |                        |                         |                             |
|------------------------|------------------------|------------------------|-------------------------|-----------------------------|
| D2=0、D1=0 A1 Light out | D4=0、D3=0 A2 Light out | D6=0、D5=0 A3 Light out | D7=0<br>Default<br>rate | D8=0<br>Can not<br>latch    |
| D2=0、D1=1 A1 Light on  | D4=0、D3=1 A2 Light on  | D6=0、D5=1 A3 Light on  |                         |                             |
| D2=1、D1=0 A1 fadein    | D4=1、D3=0 A2 fadein    | D6=1、D5=0 A3 fadein    | D7=1<br>2 times<br>rate | D8=1<br>Allowed to<br>latch |
| D2=1、D1=1 A1 fadeout   | D4=1、D3=1 A2 fadeout   | D6=1、D5=1 A3 fadeout   |                         |                             |

### Description of build-in module



Fadein module:

When a data bit is 10(D2D1 or D4D3 or D6D5) and the latch is enable, corresponding output state of LED is fadein. After get the brightest state, it will keep the state, until the new data input by effective latch.

Fadeout module:

When a data bit is 11(D2D1 or D4D3 or D6D5) and the latch is enable, corresponding output state of LED is fadeout. After the lights out, it will keep the state, until the new data input by effective latch.

Cycle time of change--T:

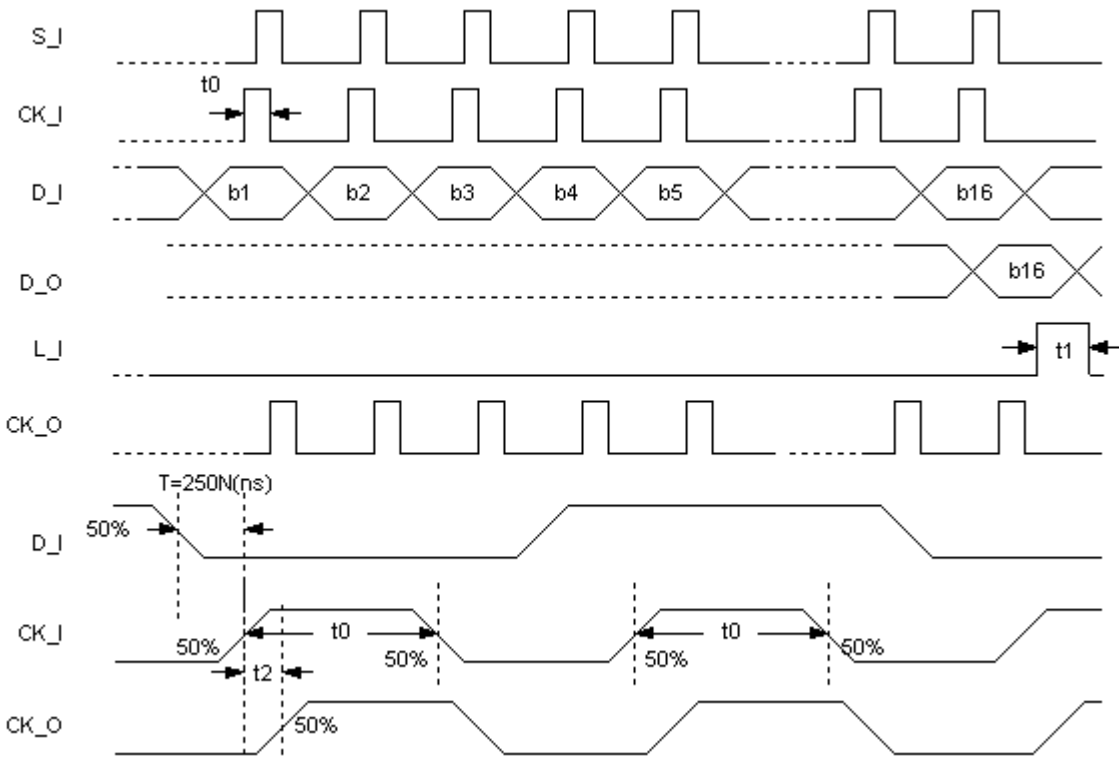
When D7=0,  $T = T_{zc} \times 128$  set ,series is 128. For example: When  $Zc=50\text{Hz}$ ,  $T=2.56\text{s}$ , if every latch is effective, fadein/fadeout module will resume the change.

### Electric parameter ( $V_{DD}=5\text{V}$ , temperature= $25^\circ\text{C}$ )

| ITEM  | SYMBOL   | TEST CONDITIONS                                 | MIN. | TYP. | MAX. | UNIT             |
|---|----------|---|------|------|------|------------------|
| Threshold voltage of output tube                | $V_{OL}$ | $I_{DS} \leq 1\mu\text{A}$ , $V_{DD}=5\text{V}$ | --   | --   | 6    | V                |
| Operating voltage                               | $V_{CC}$ | Stable and functioning properly                 | 3    | 5    | 5.5  | V                |
| Operating current                               | $I_{CC}$ | $V_{DD}=5\text{V}$ , oscillations, no load      | --   | 200  | 400  | $\mu\text{A}$    |
| DATA input, changes of high level and low level | $V_{IN}$ | Stable and functioning properly                 | 3.8  | --   | 6    | V                |
| Output current of drive                         | $I_{OL}$ | $V_{DD}=5\text{V}$ , $V_{DS}=0.8\text{V}$       | --   | 30   | --   | mA               |
| Output current of buffer                        | $I_{OH}$ | $V_{DD}=5\text{V}$ , $V_{DS}=-0.8\text{V}$      | --   | 5    | --   | mA               |
|   | $I_{OL}$ | $V_{DD}=5\text{V}$ , $V_{DS}=0.8\text{V}$       | --   | 10   | --   | mA               |
| temperature                                     | Temp     |   | 0    | 25   | 70   | $^\circ\text{C}$ |
| Work frequency of terminal-S                    | $F_s$    | $V_{DD}=5\text{V}$                              |      |      | 200  | Hz               |

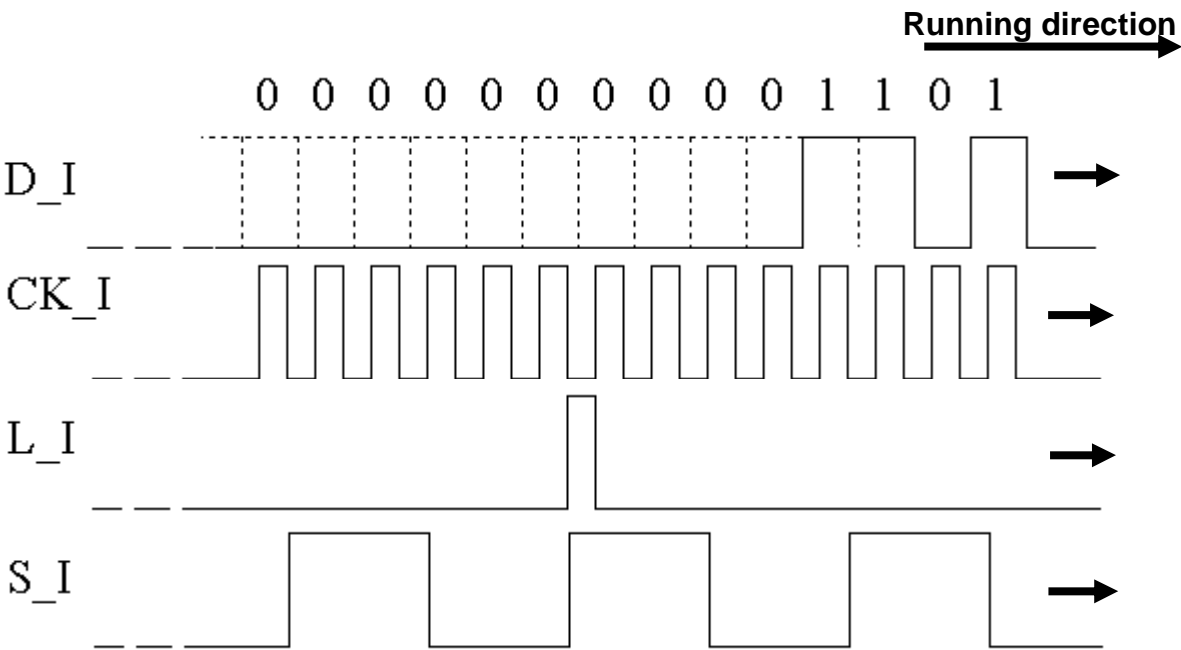
**Timing diagram(entry data from high level)**

$t_0 \geq 300\text{ns}$  ;  $t_1 \geq 1\mu\text{s}$ ;  $T \geq 250N(\text{ns})$ , N: the number of cascade;  $t_2 \approx 100\text{ns}$ .



**Impression Drawing & Data Format**

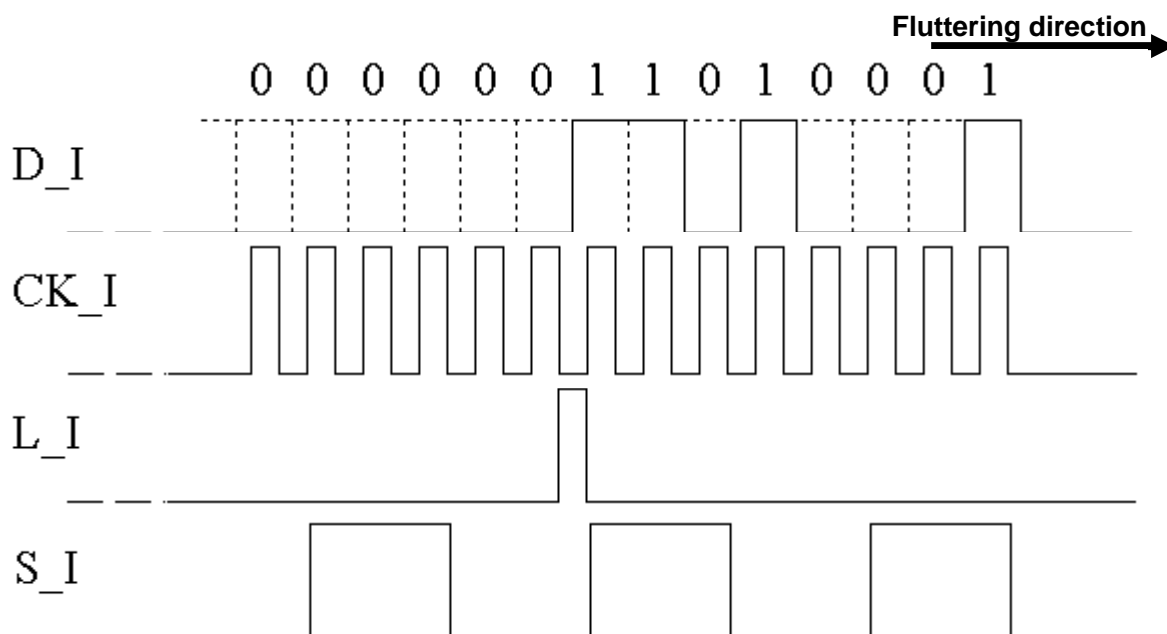
**1. Monochrome , one-way, gradually run**



Description: There is a "gradual change" mode in HL1606, so D\_I only need one set of data "10110000", then input "0" to the end is okay. Clock signal has been sent to CK\_I, sent a "1" to L\_I after 8 clock signal. Change once the signal of S\_I, the output decline in a series. A clock cycle in S\_I, output is keep in 512Hz refresh frequency, to maintain the same level(series) of output duty cycle refresh. If no data sent to S\_I,

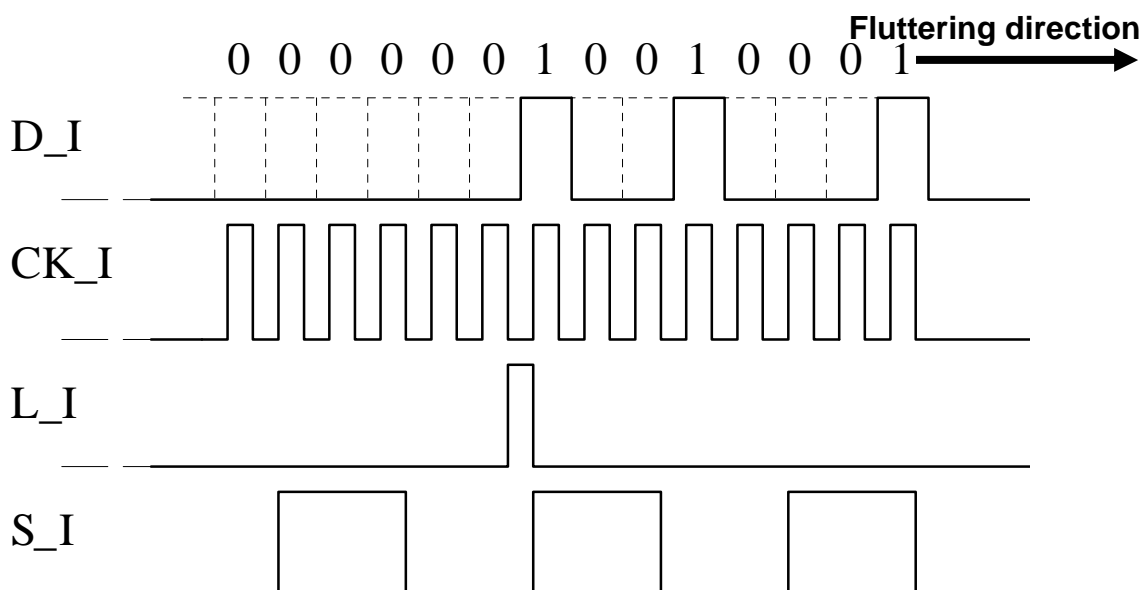
output will remain the same duty cycle refresh.

## 2. Colorful fluttering



Description: There is a “gradual change” mode in HL1606, so D\_I only need one set of data “10001011”, then input “0” to the end is okay (red to green gradually). Clock signal has been sent to CK\_I, sent a “1” to L\_I after 8 clock signal. Change once the signal of S\_I, the output series change once. A clock cycle in S\_I, output is keep in 512Hz refresh frequency, to maintain the same level (series) of output duty cycle refresh. If no data sent to S\_I, output will remain the same duty cycle refresh. Just finished in a color change, change the data of D-I.

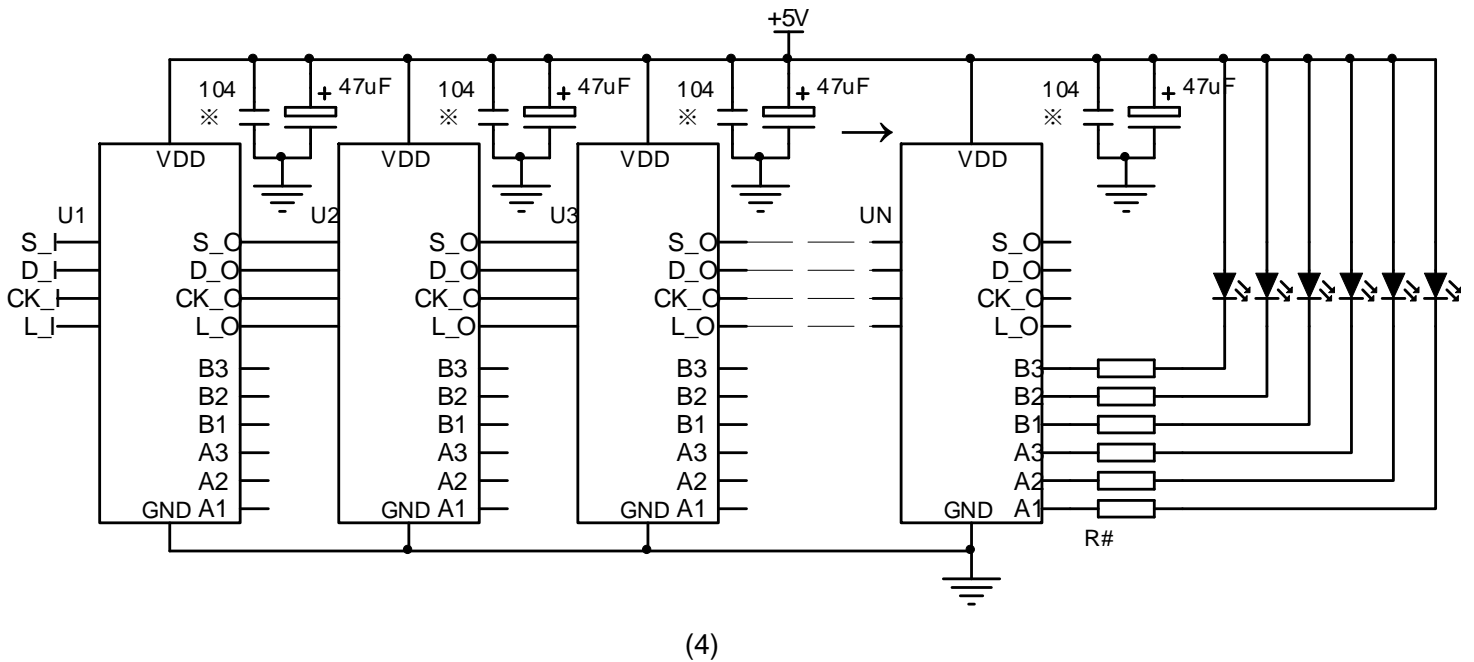
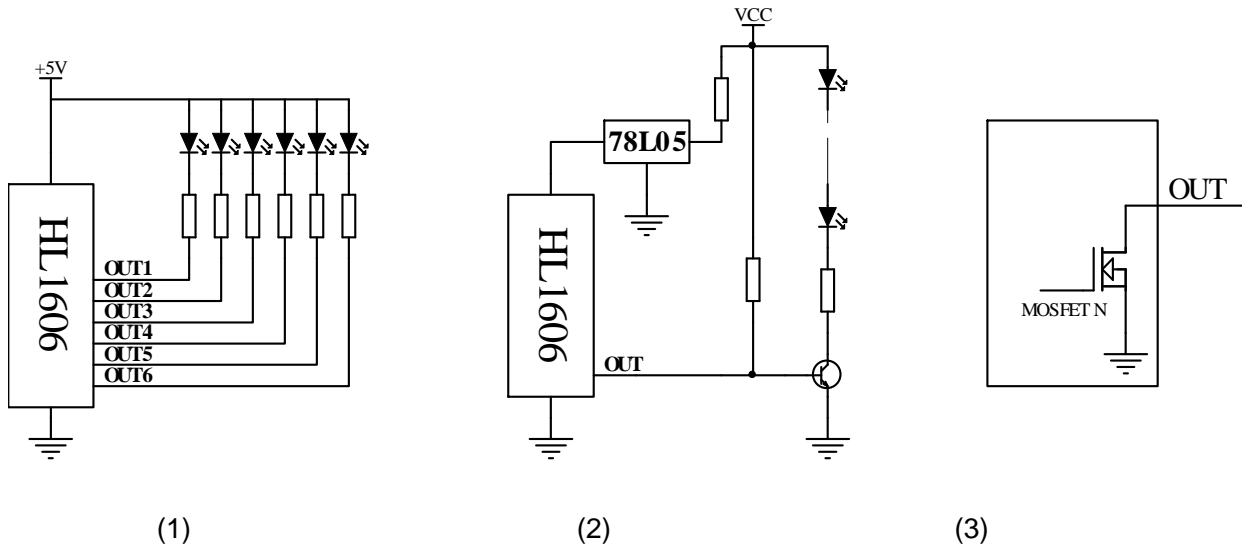
## 3. Full-color fluttering



Description: There is a “gradual change” mode in HL1606, so D\_I only need one set of data “10001001”,

then input "0" to the end is okay(red to yellow gradually). Clock signal has been sent to CK\_I, sent a "1" to L\_I after 8 clock signal. Change once the signal of S\_I, the output series change once. A clock cycle in S\_I, output is keep in 512Hz refresh frequency, to maintain the same level(series) of output duty cycle refresh. If no data sent to S\_I, output will remain the same duty cycle refresh. Just finished in a color change, change the data of D-I.

## Application



## Application Notes

1. Picture(1), 1<sup>st</sup> connection method: triode will not connect to output of IC, output current reach 30Ma, output can connect to two-ways, ensure that the output voltage must be less than 6V.
2. Picture(2), 2<sup>nd</sup> connection method: triode connect to output of IC. Because the NPN-type transistor at the base took on the extreme pull-up resistor, the "output duty cycle of IC" and the "LED brightness" is inversely proportional to. When the IC doesn't output, the transistor fully conducting, LED full-bright.

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3. Picture (3), internal structure of the “output port of IC”. The output is NMOS open-drain output.
  4. Picture (4), application drawing of cascade. Connection method of output termination (U1-UN) is same. Ceramic capacitor “※” should be as close as possible to the chip, and work before the power input to the IC. Resistance “#” is adjustable, adjust the brightness of LED by adjust the value of resistance, and then we can get different blending effect. When the IC work, first into the highest, then into the low, the output is after the drive of “chip control signal”, this output can be used as the input signal of back-end circuit.