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GALILEO GEN2

INTEL QUARK X1000

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FAB H

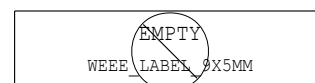
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PBA: H48125-800

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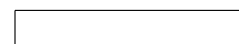
LB1



WEEE

LB6V1

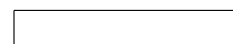
LABEL



1500X500_TARGET
SERIAL NUMBER

LB3

LABEL



1375X250_TARGET
MAC ADDRESS LABEL

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Wed May 21 10:12:25 2014

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		
TITLE	GALILEO Gen2	DOCUMENT NUMBER
	DESIGN TITLE PAGE	H38681
		REV
		2.0
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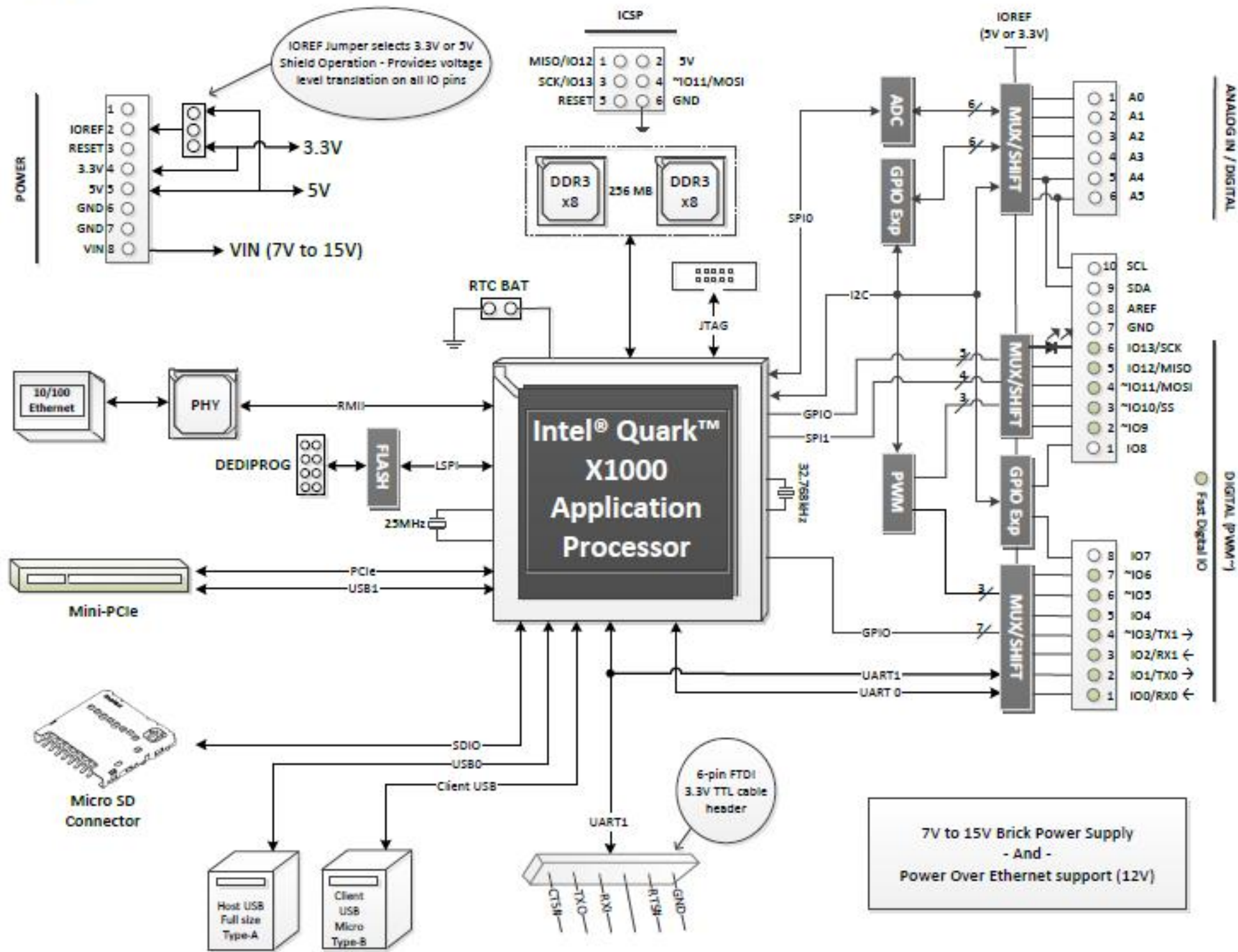
Intel® Galileo Design Document

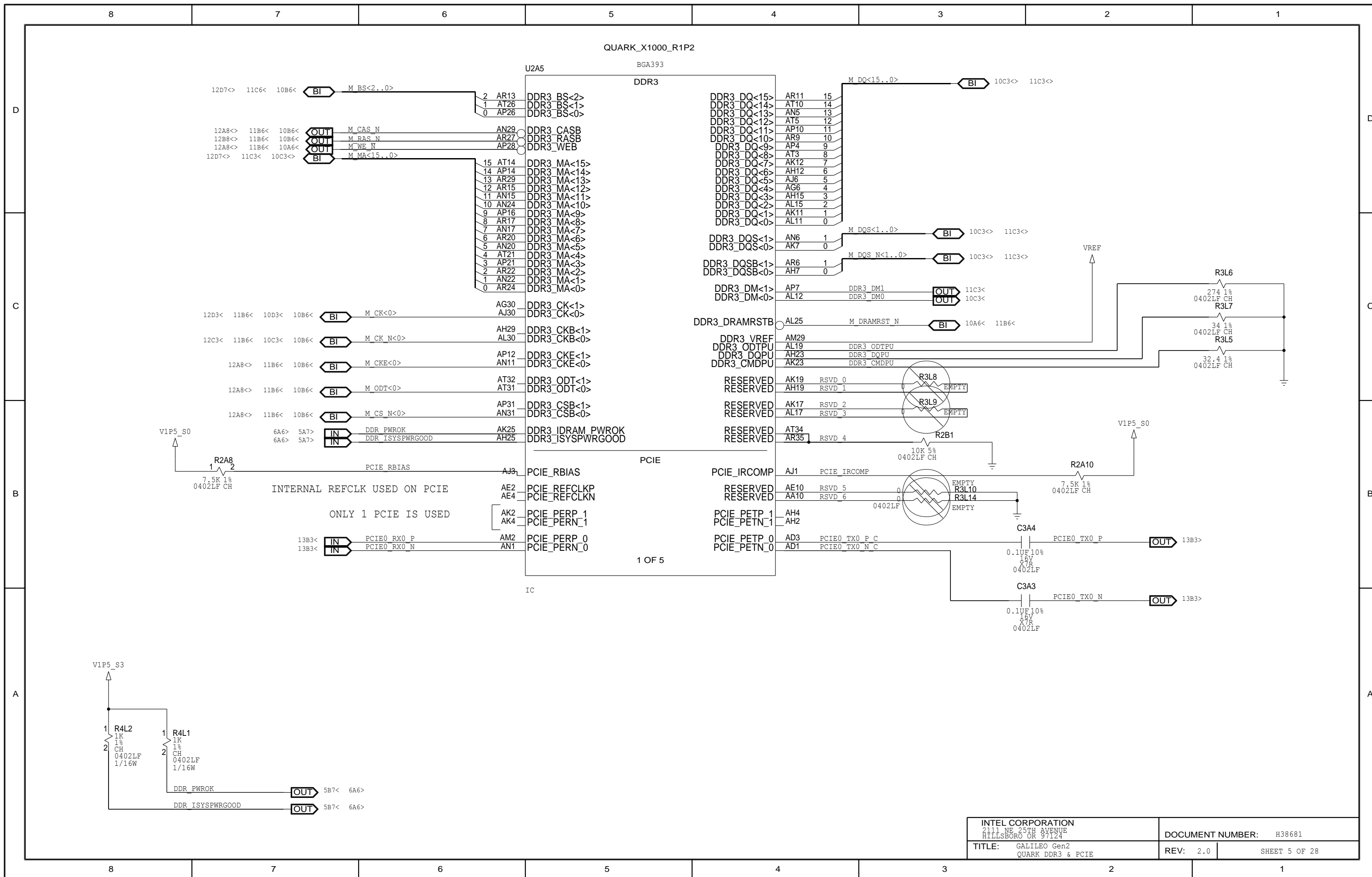
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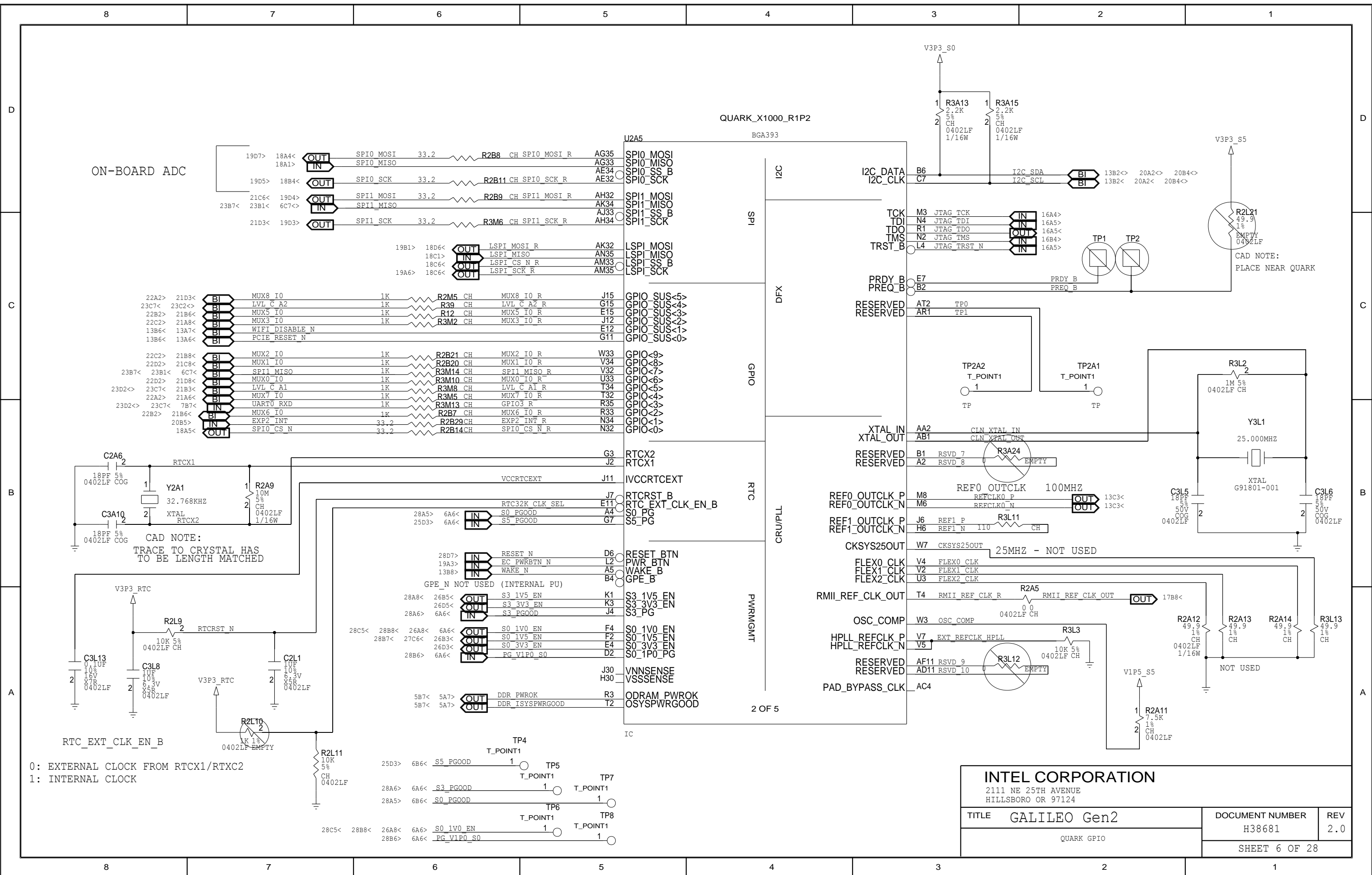
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INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 DISCLAIMER		REV: 2.0	SHEET 3 OF 28

Intel® Galileo™ Board Fab H (PVT)
May/2014

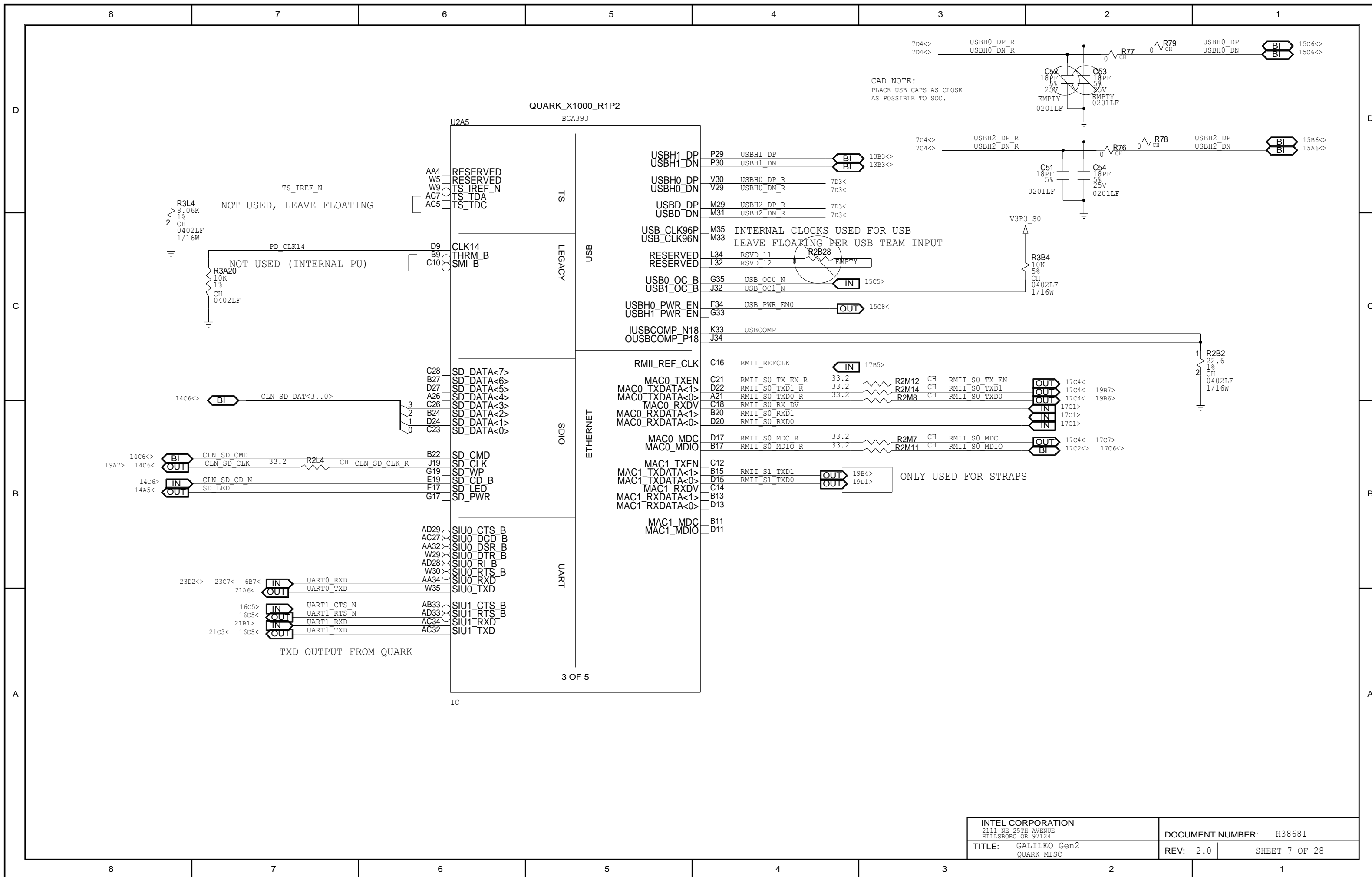


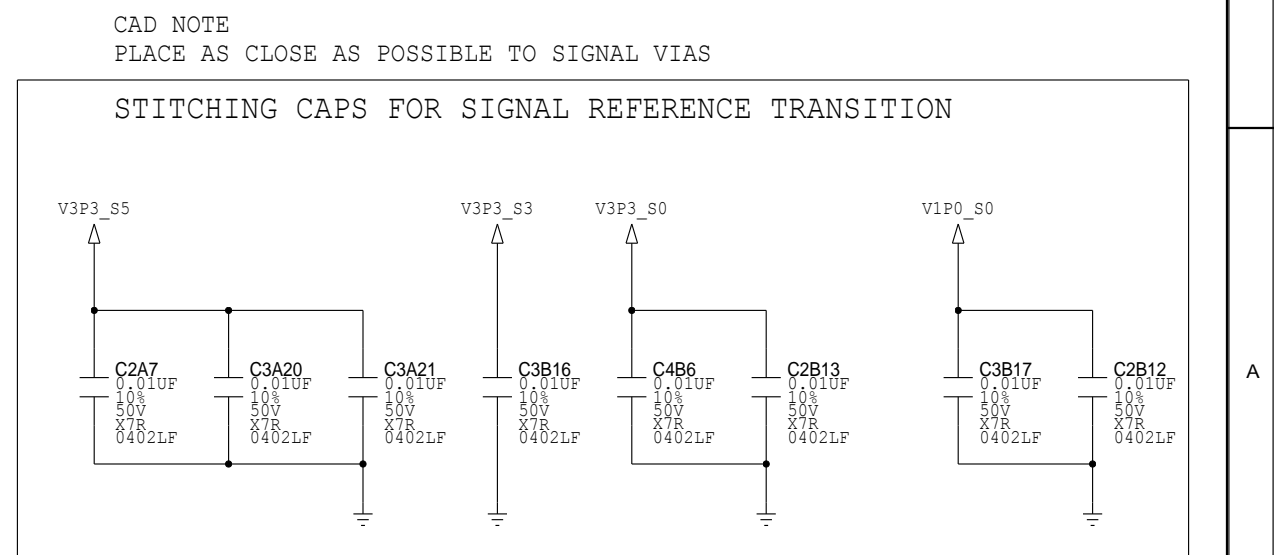
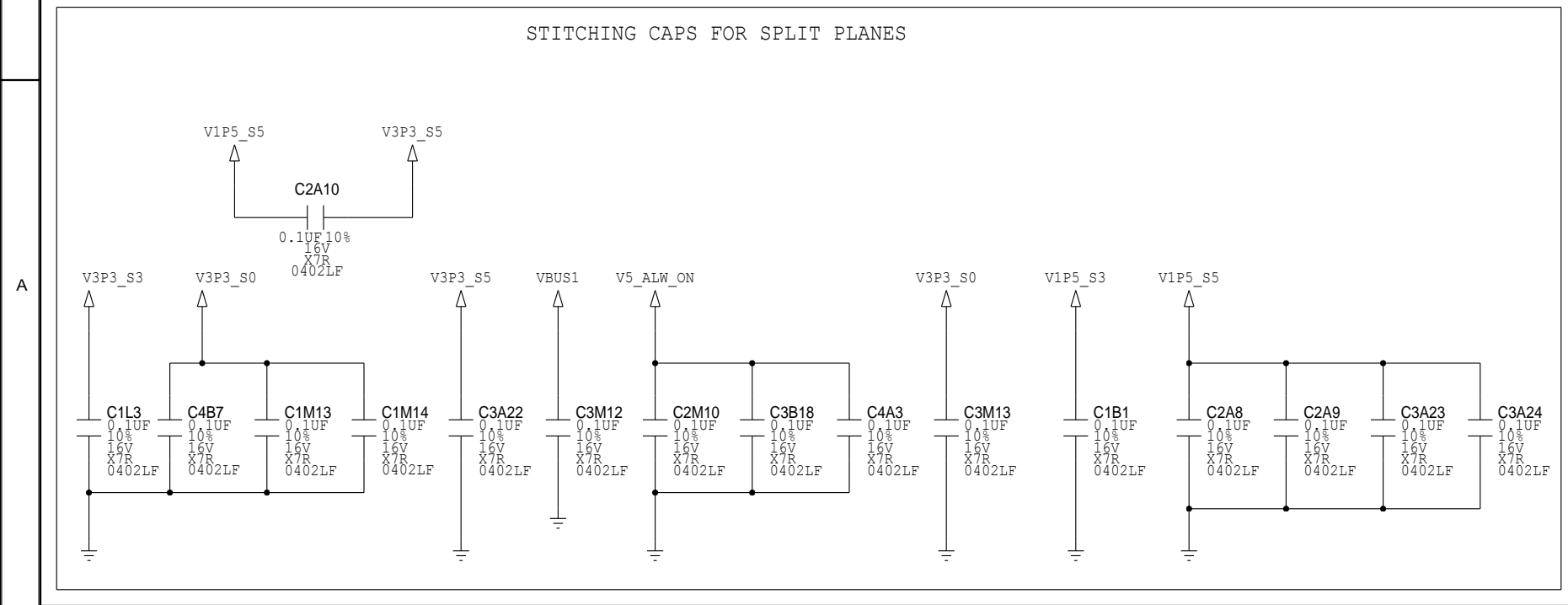
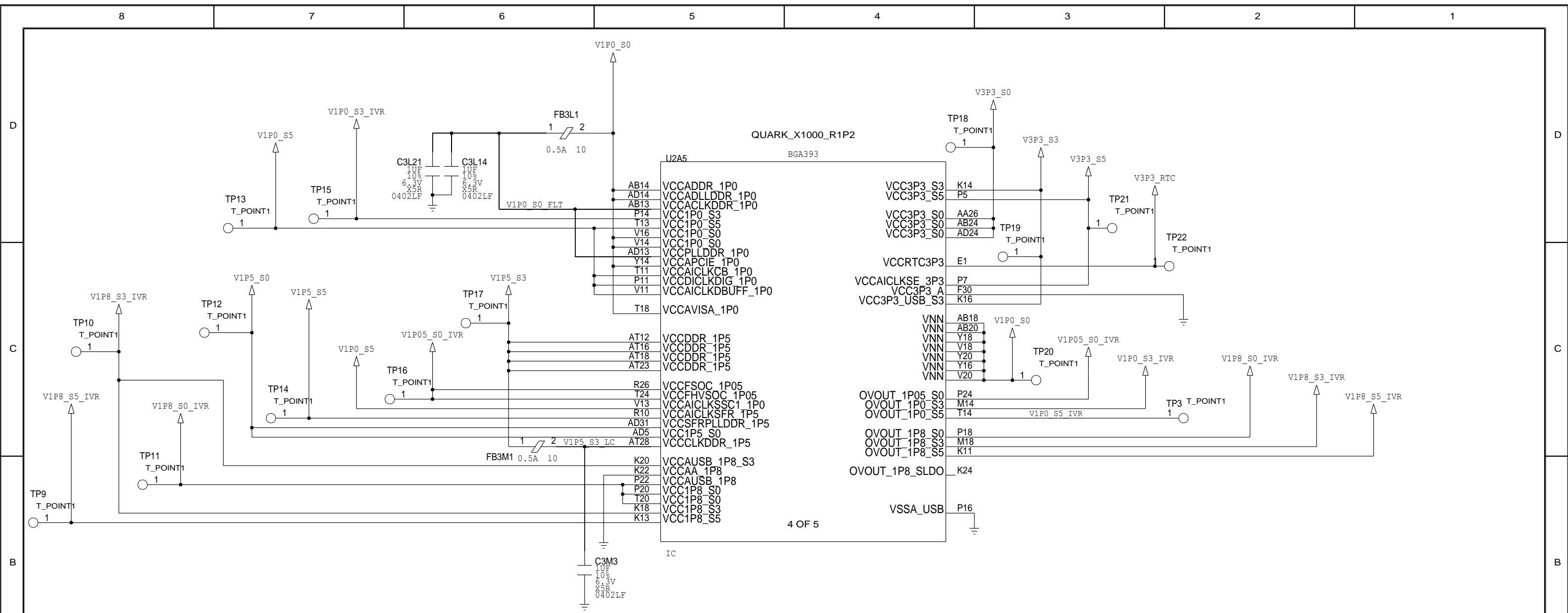




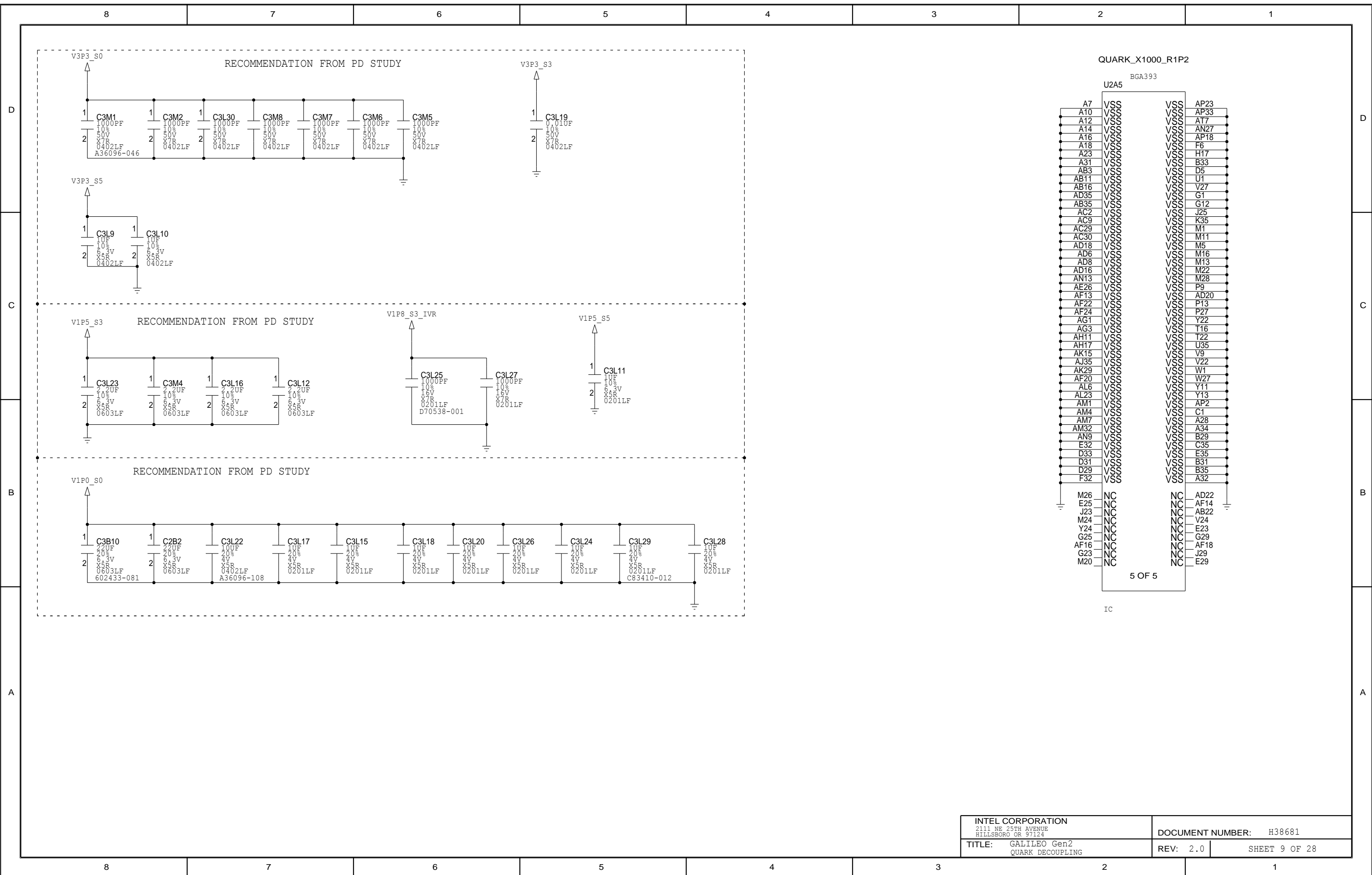
INTEL CORPORATION
 2111 NE 25TH AVENUE
 HILLSBORO OR 97124

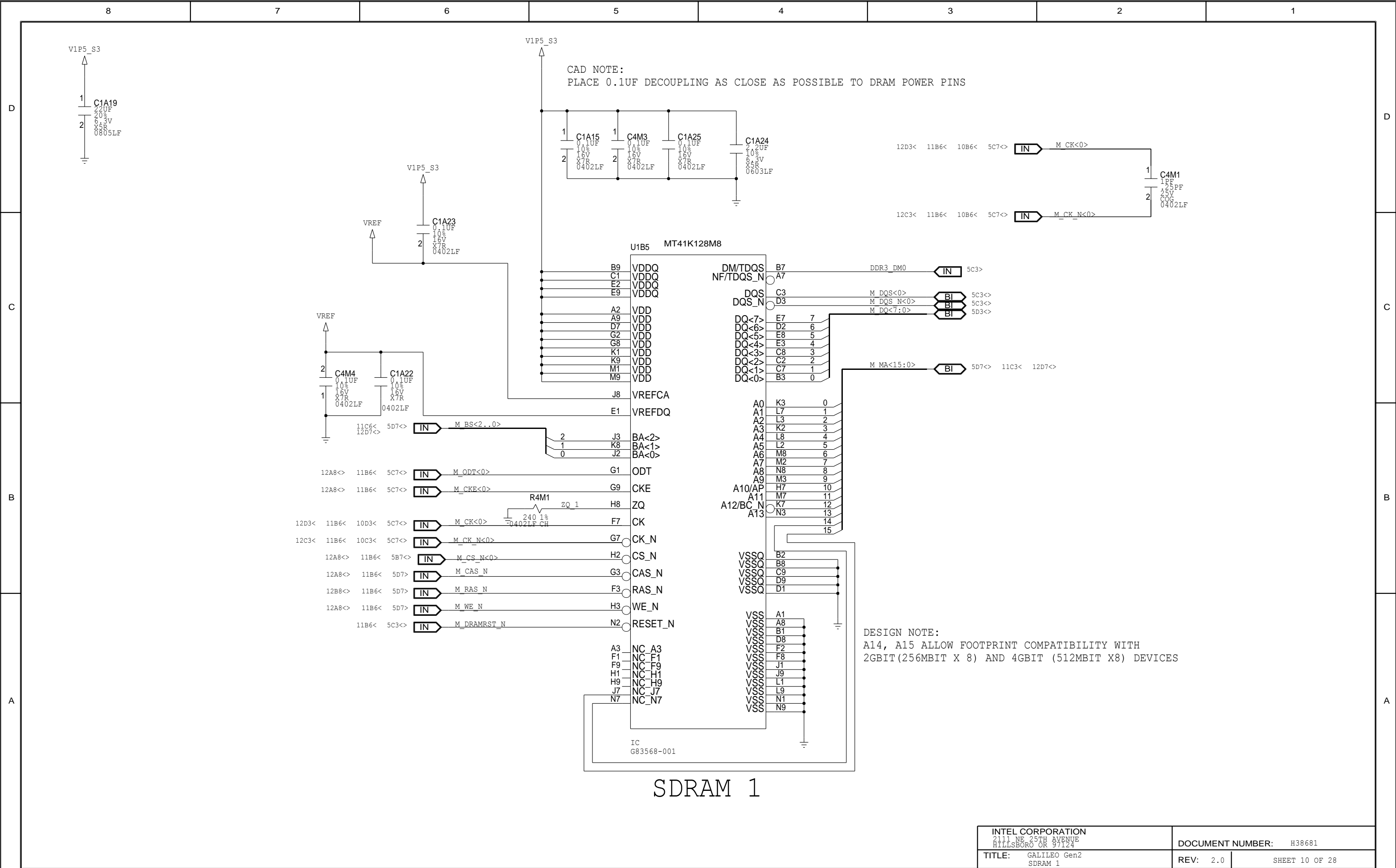
TITLE	GALILEO Gen2	DOCUMENT NUMBER	H38681	REV	2.0
QUARK GPIO			SHEET 6 OF 28		



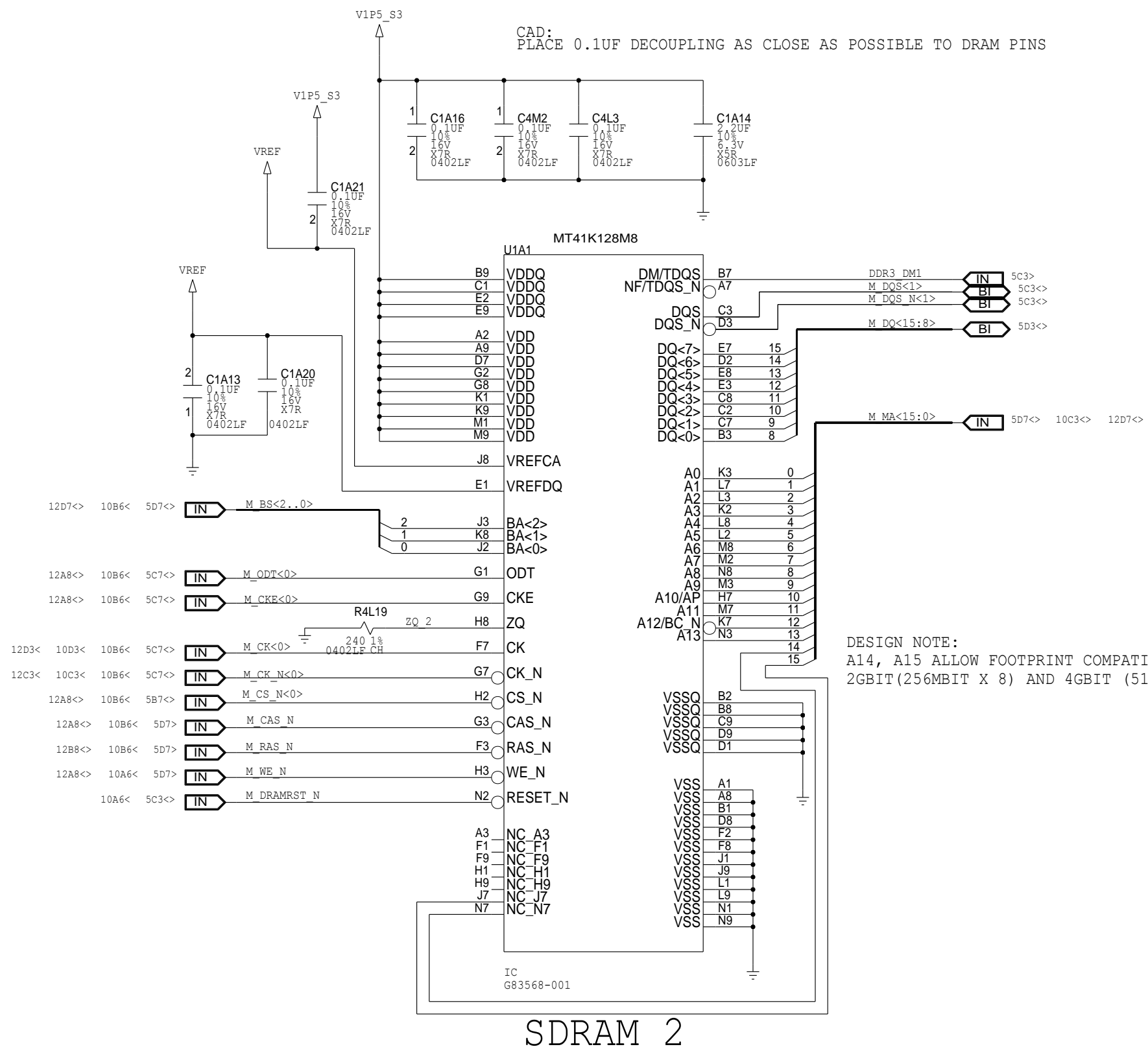


CAD NOTE
PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS

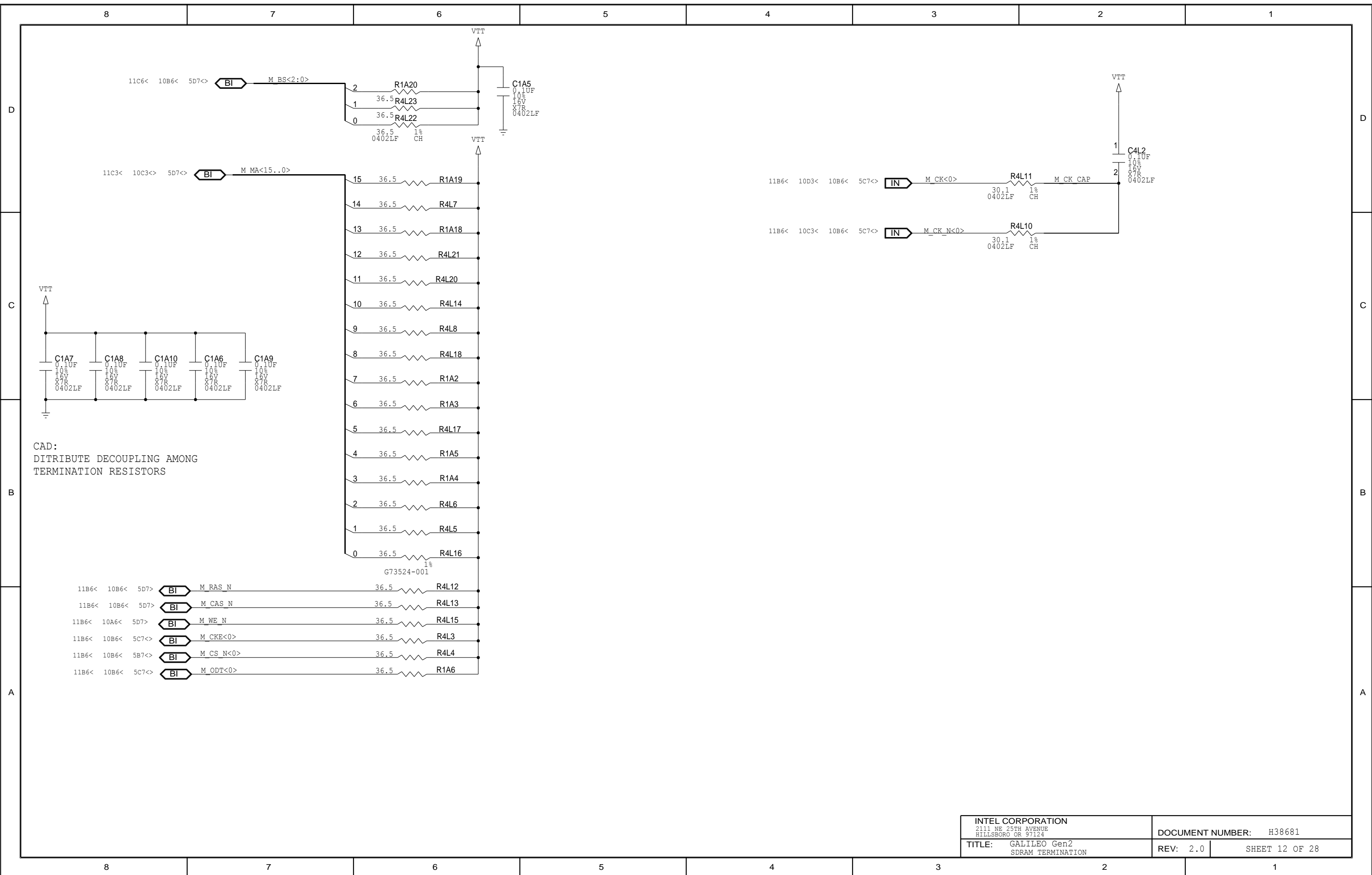




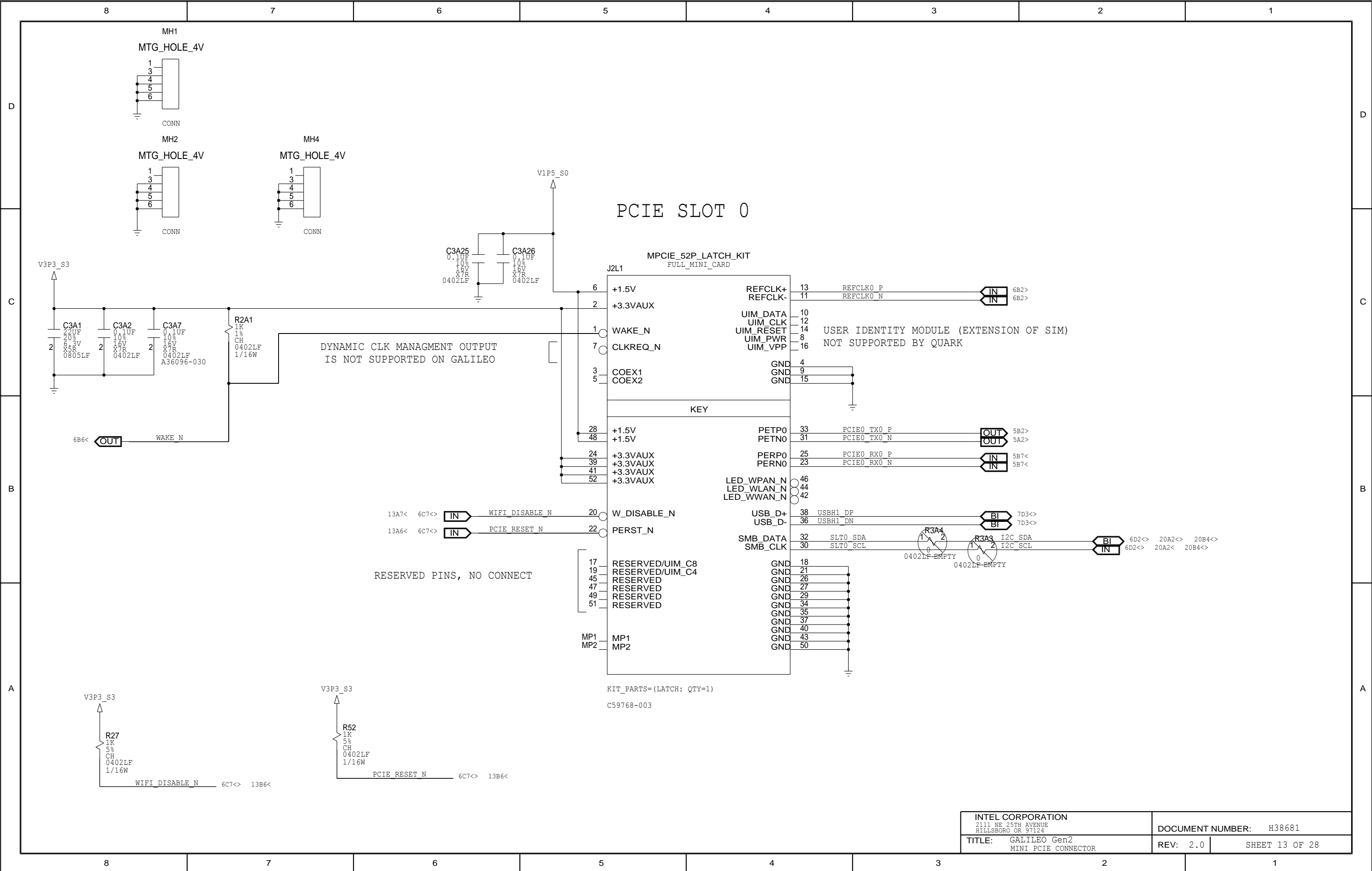
SDRAM 1

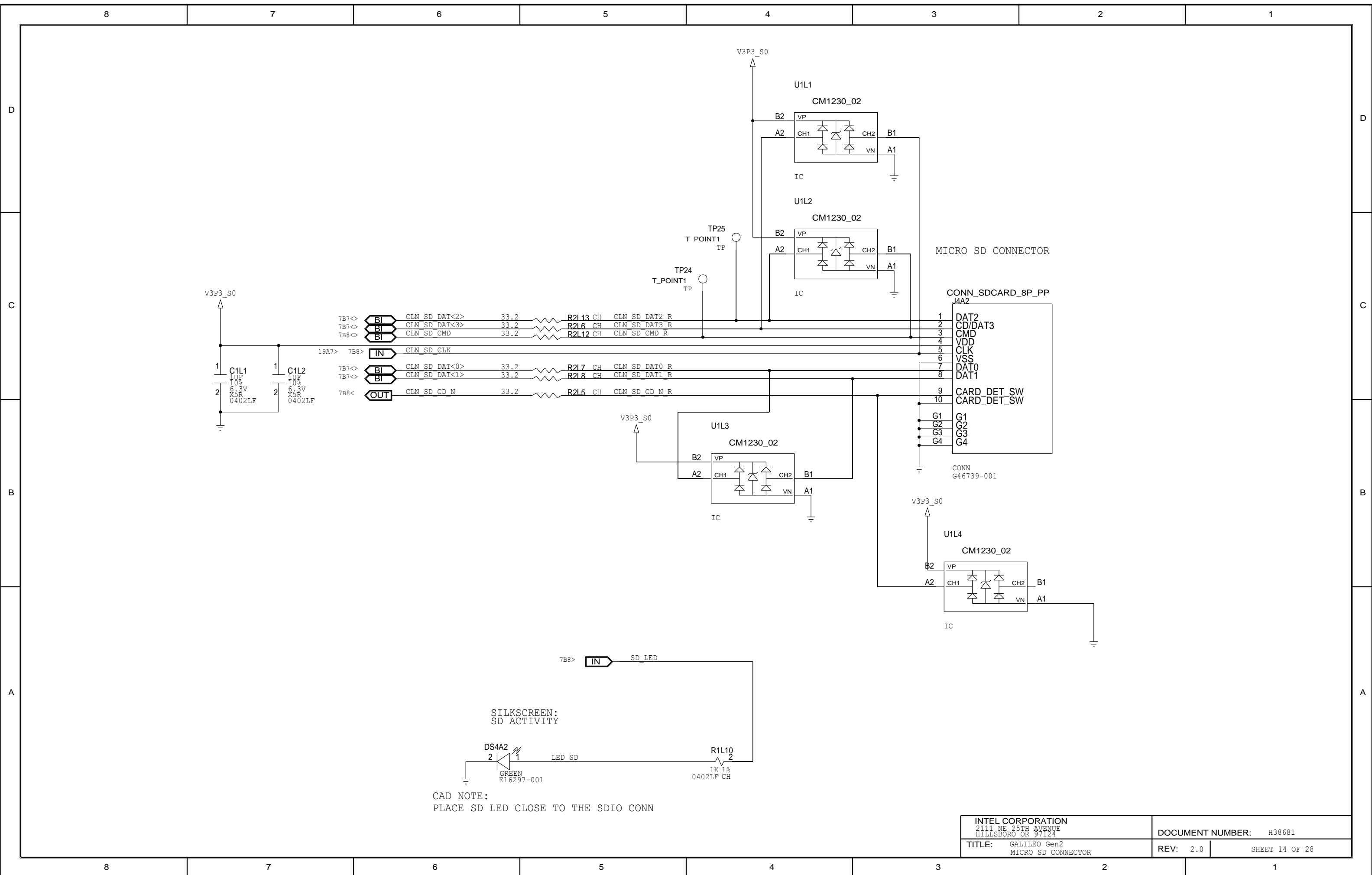


DESIGN NOTE:
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH
2GBIT(256MBIT X 8) AND 4GBIT (512MBIT X8) DEVICES



CAD:
DITRIBUTE DECOUPLING AMONG
TERMINATION RESISTORS





7B7<	BI	CLN_SD_DAT<2>	33.2	R21.13 CH	CLN_SD_DAT2 R
7B7<	BI	CLN_SD_DAT<3>	33.2	R21.6 CH	CLN_SD_DAT3 R
7B8<	BI	CLN_SD_CMD	33.2	R21.12 CH	CLN_SD_CMD R
19A7>	IN	CLN_SD_CLK			
7B7<	BI	CLN_SD_DAT<0>	33.2	R21.7 CH	CLN_SD_DAT0 R
7B7<	BI	CLN_SD_DAT<1>	33.2	R21.8 CH	CLN_SD_DAT1 R
7B8<	OUT	CLN_SD_CD_N	33.2	R21.5 CH	CLN_SD_CD_N R

MICRO SD CONNECTOR

1	DAT2
2	CD/DAT3
3	CMD
4	VDD
5	CLK
6	VSS
7	DAT0
8	DAT1
9	CARD_DET_SW
10	CARD_DET_SW
G1	G1
G2	G2
G3	G3
G4	G4

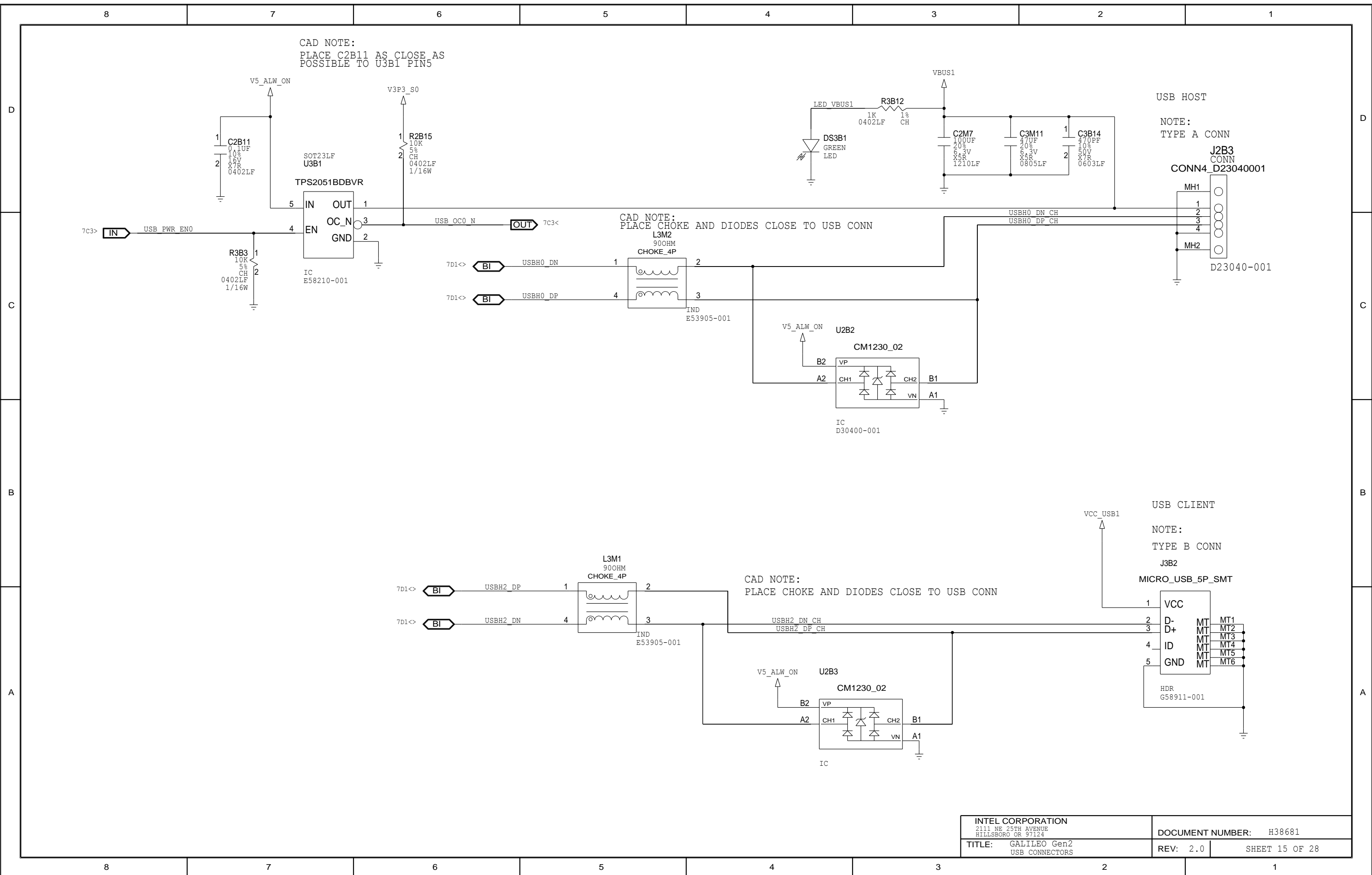
CONN_SDCARD_8P_PP J4A2

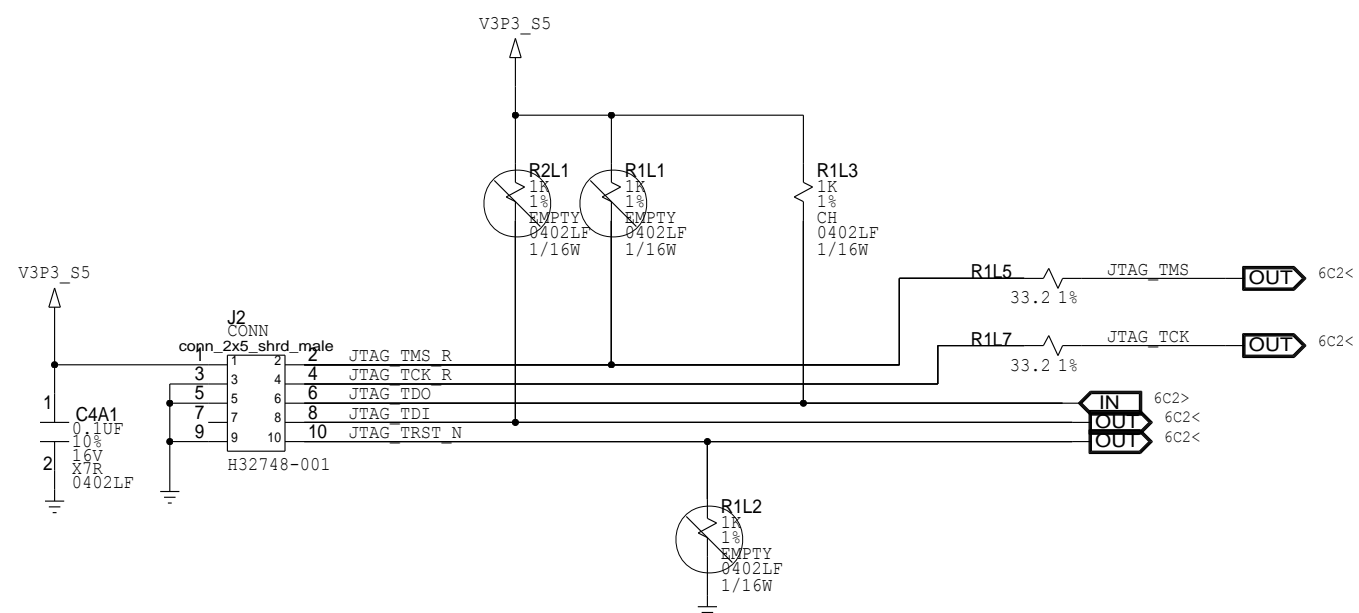
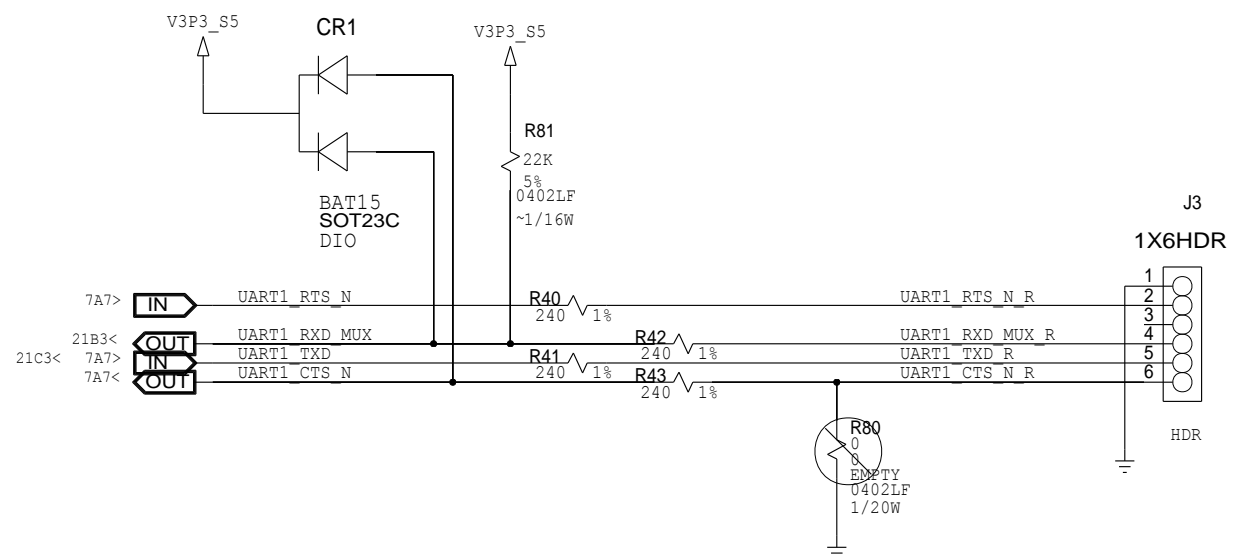
CONN G46739-001

SILKSCREEN:
SD ACTIVITY

CAD NOTE:
PLACE SD LED CLOSE TO THE SDIO CONN

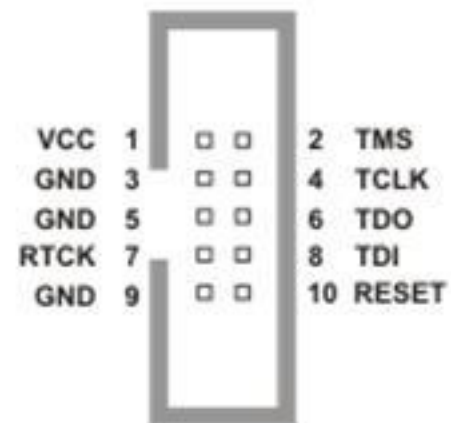
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 MICRO SD CONNECTOR		REV: 2.0	SHEET 14 OF 28



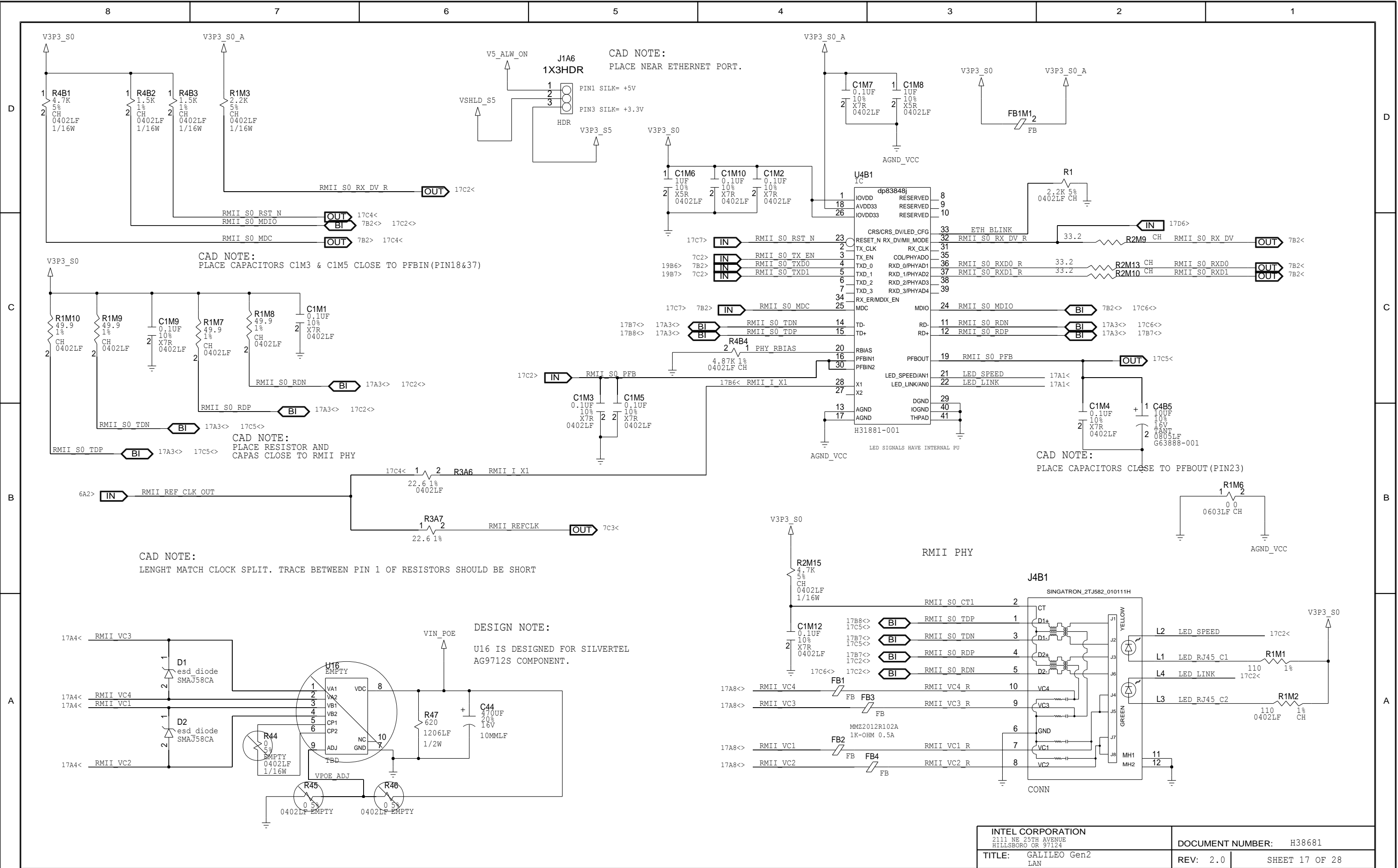


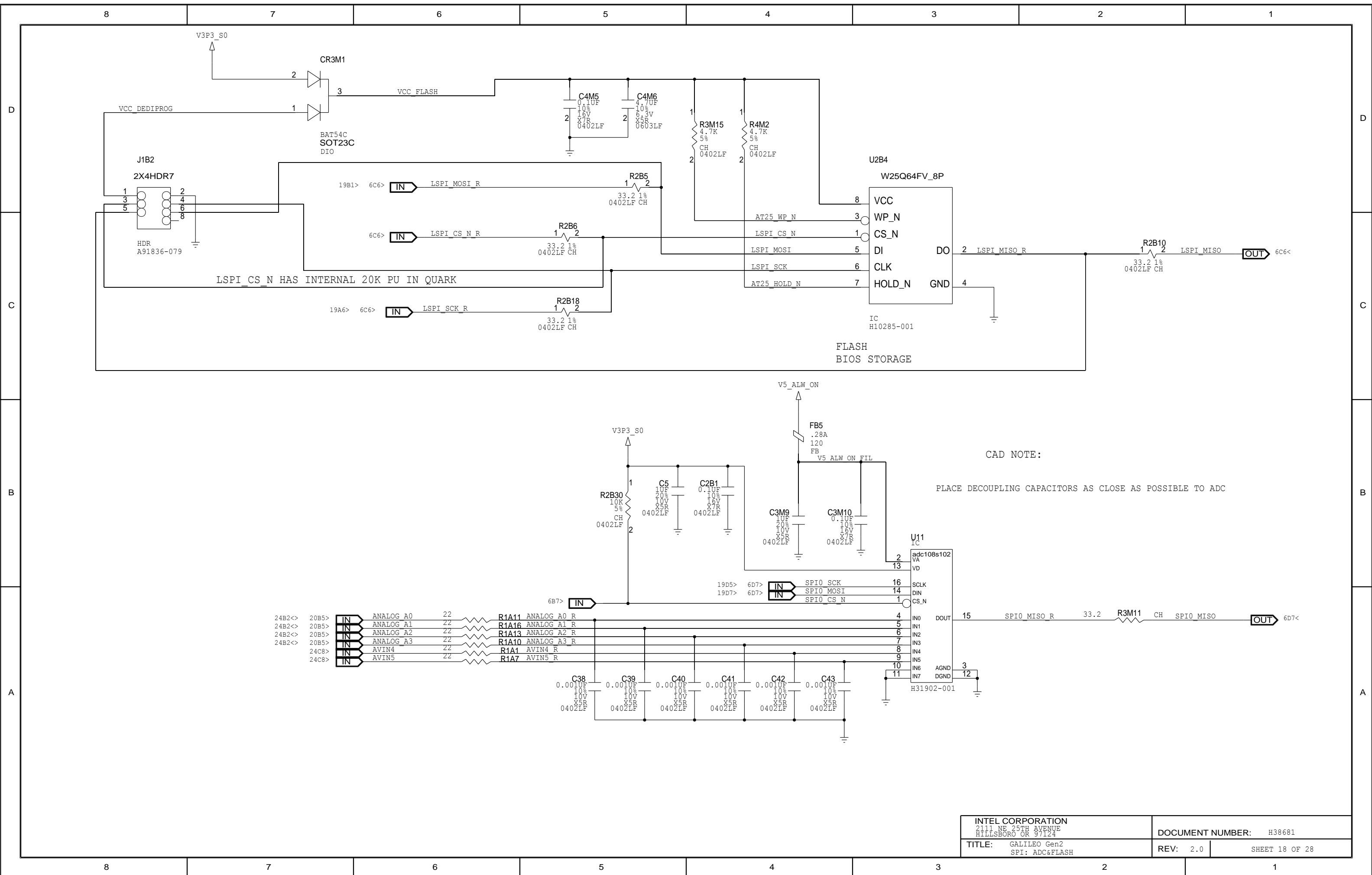
CAD NOTE:
PLACE CONNECTOR ON SOLDER-SIDE.

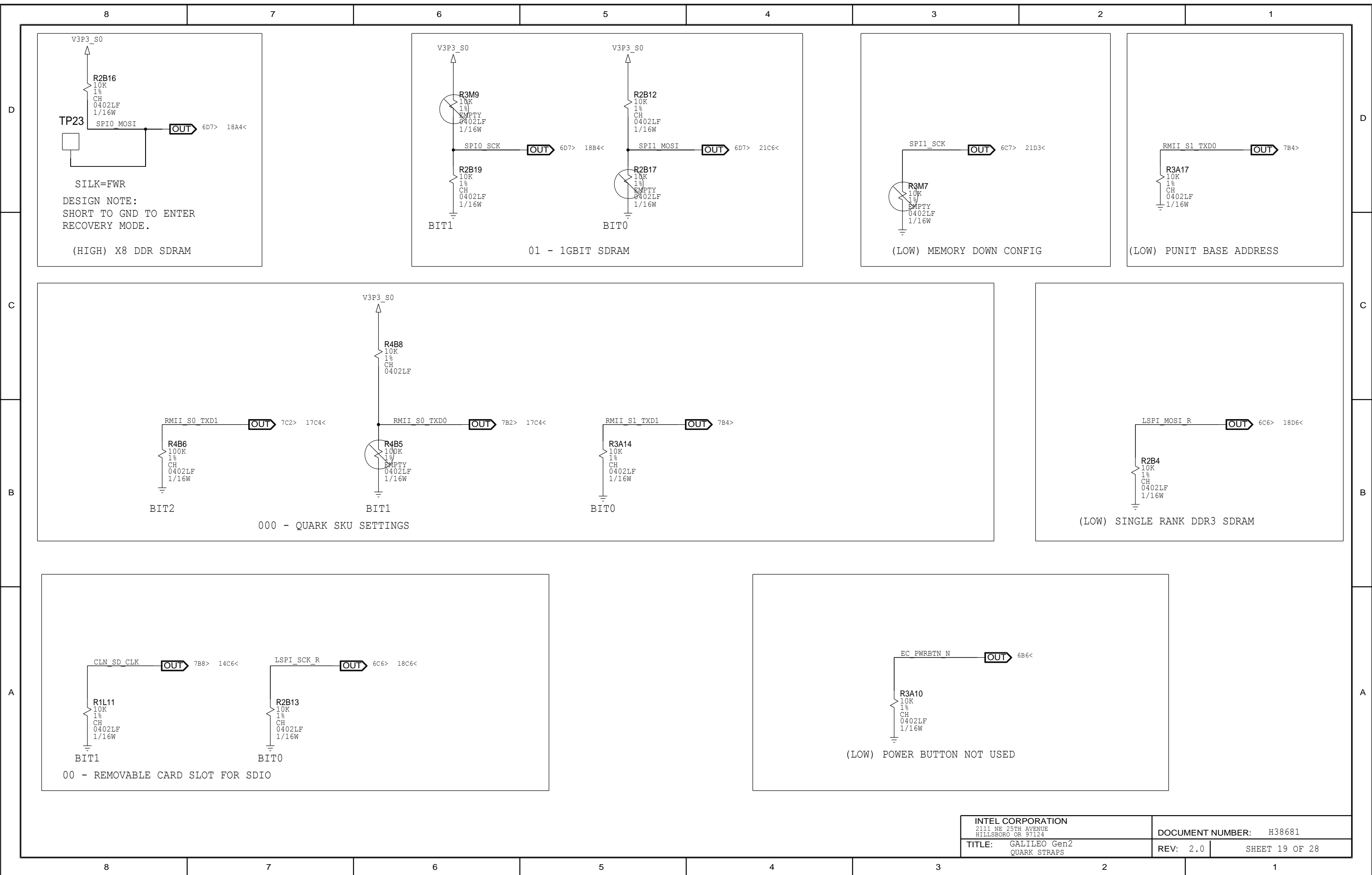
MINI-JTAG CONNECTOR

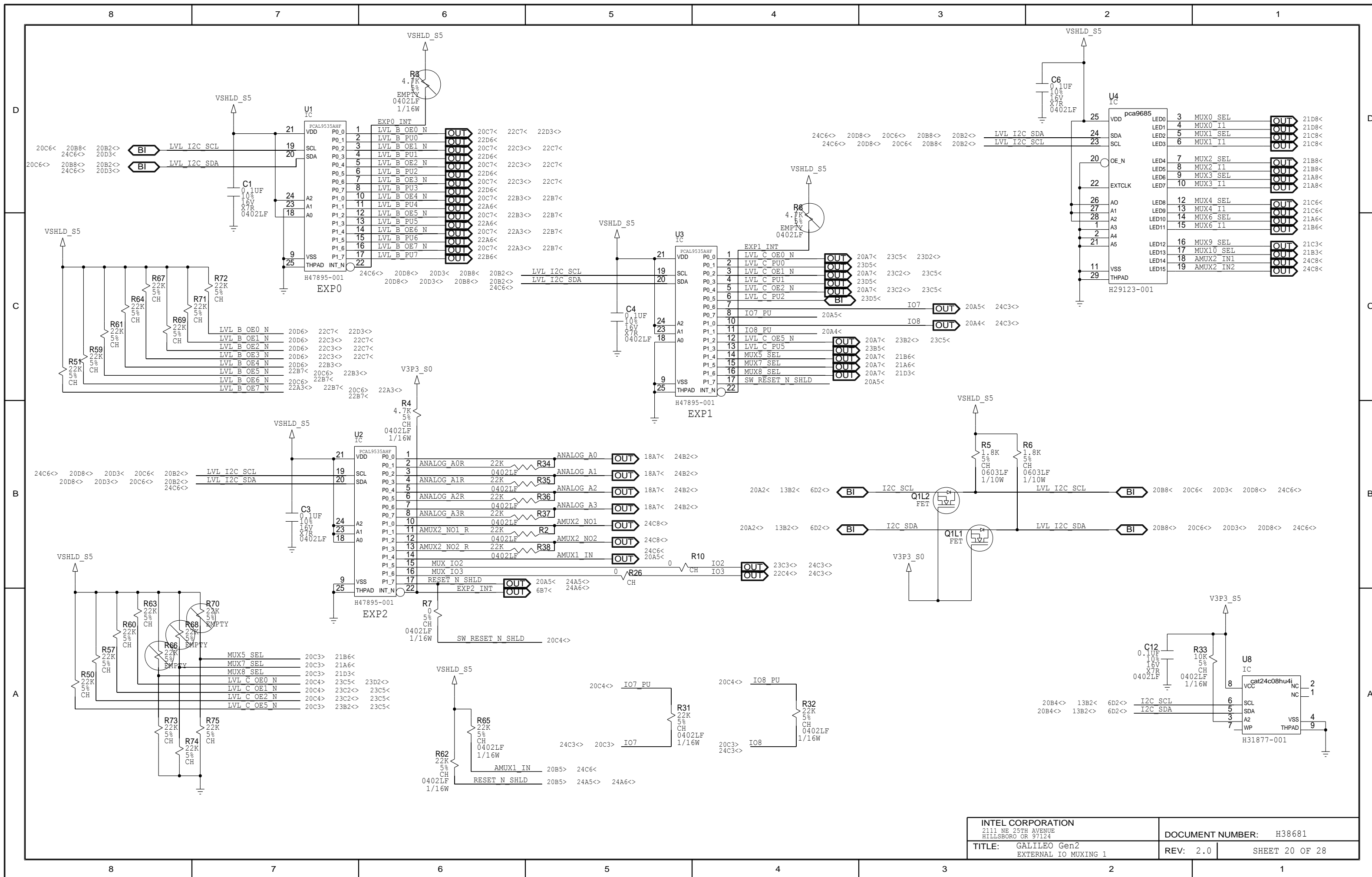


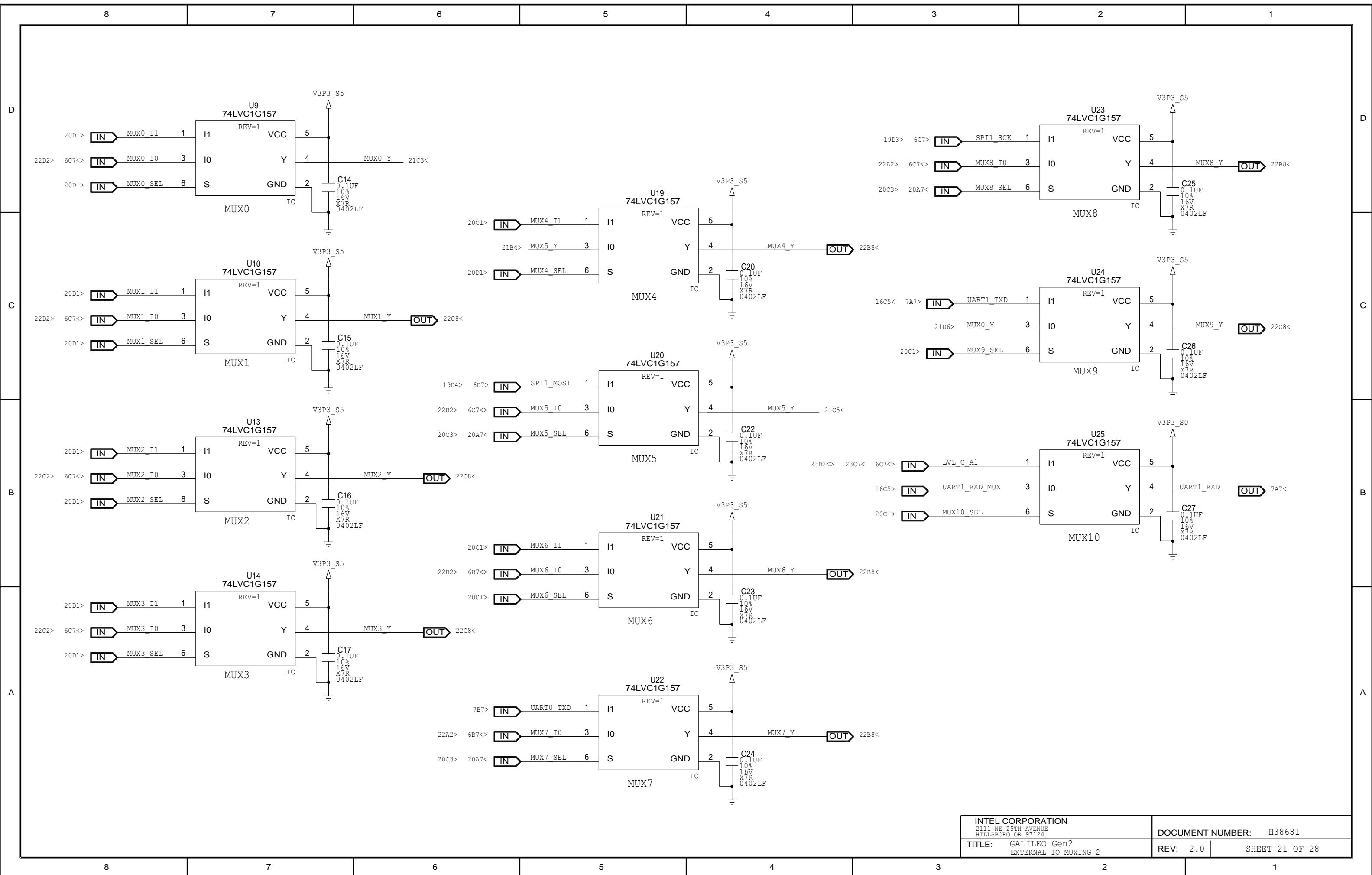
INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 UART 1 & JTAG		REV: 2.0	SHEET 16 OF 28

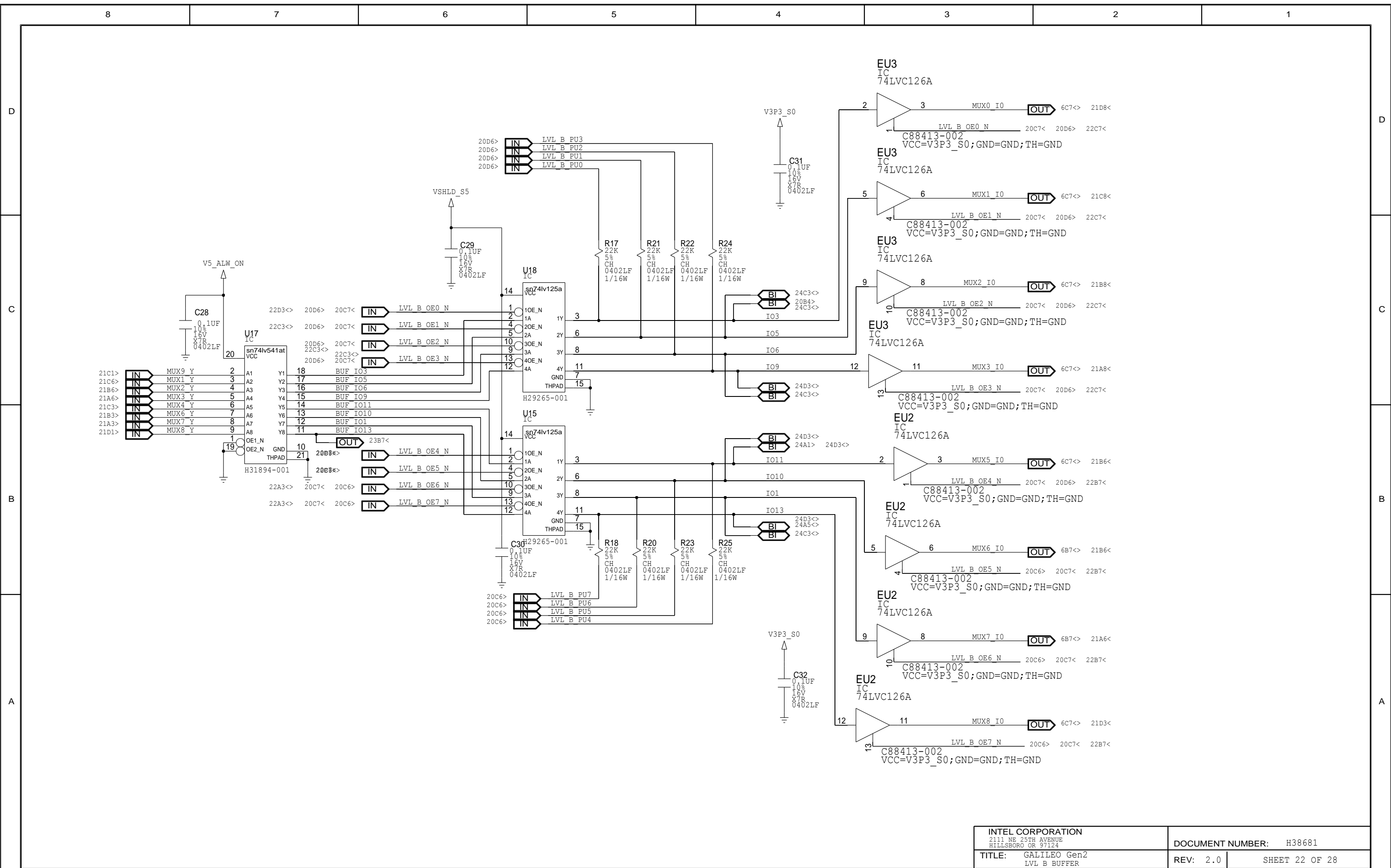


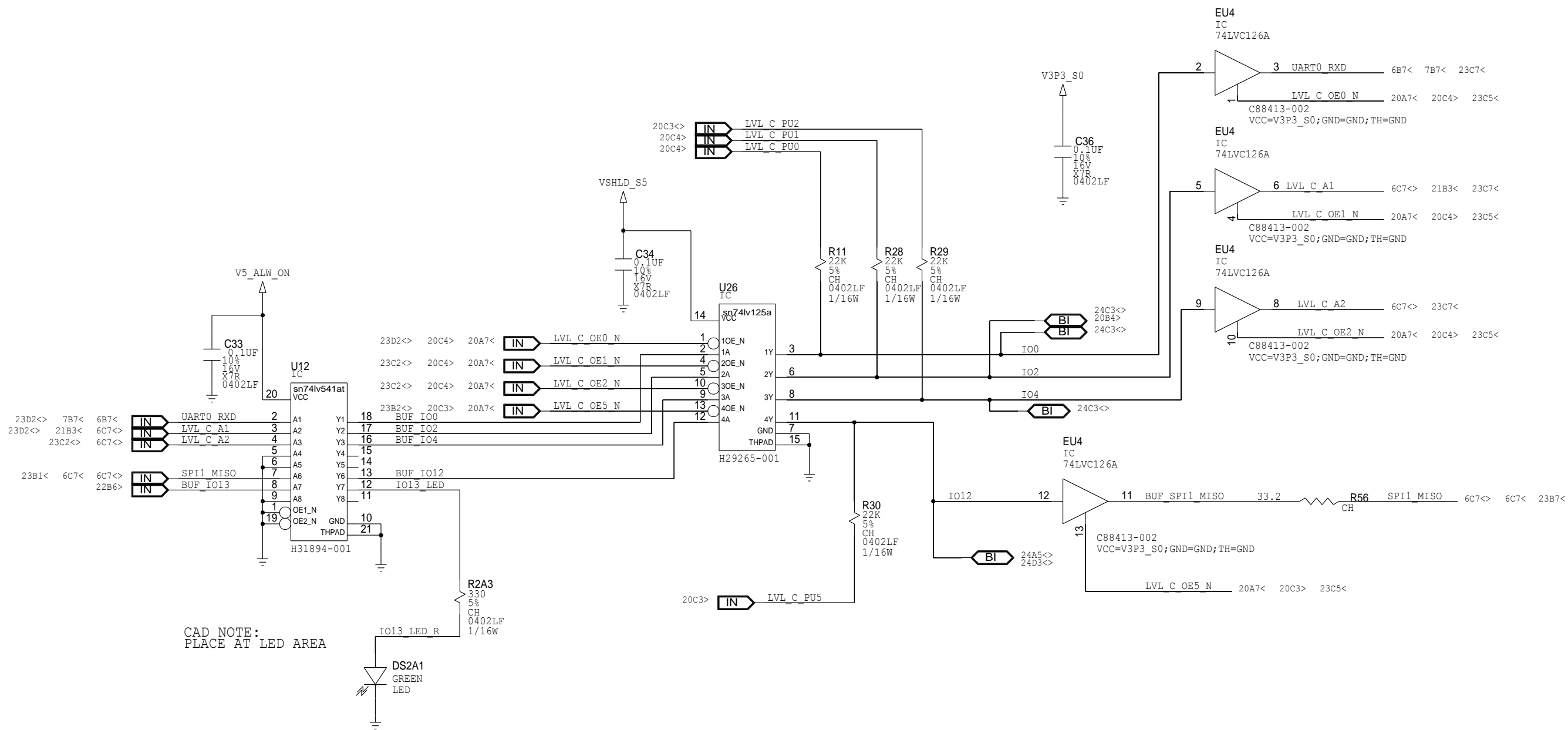




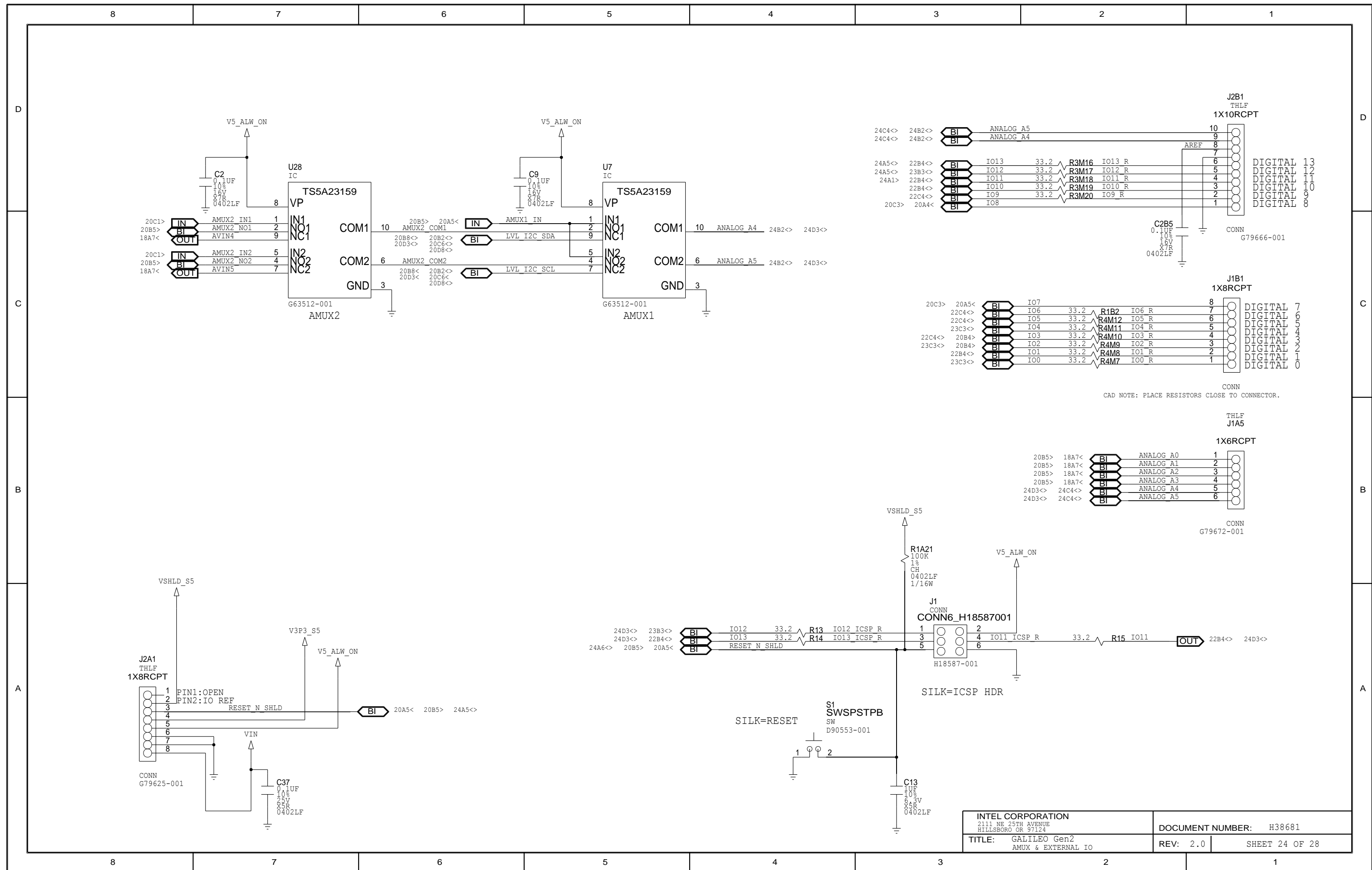


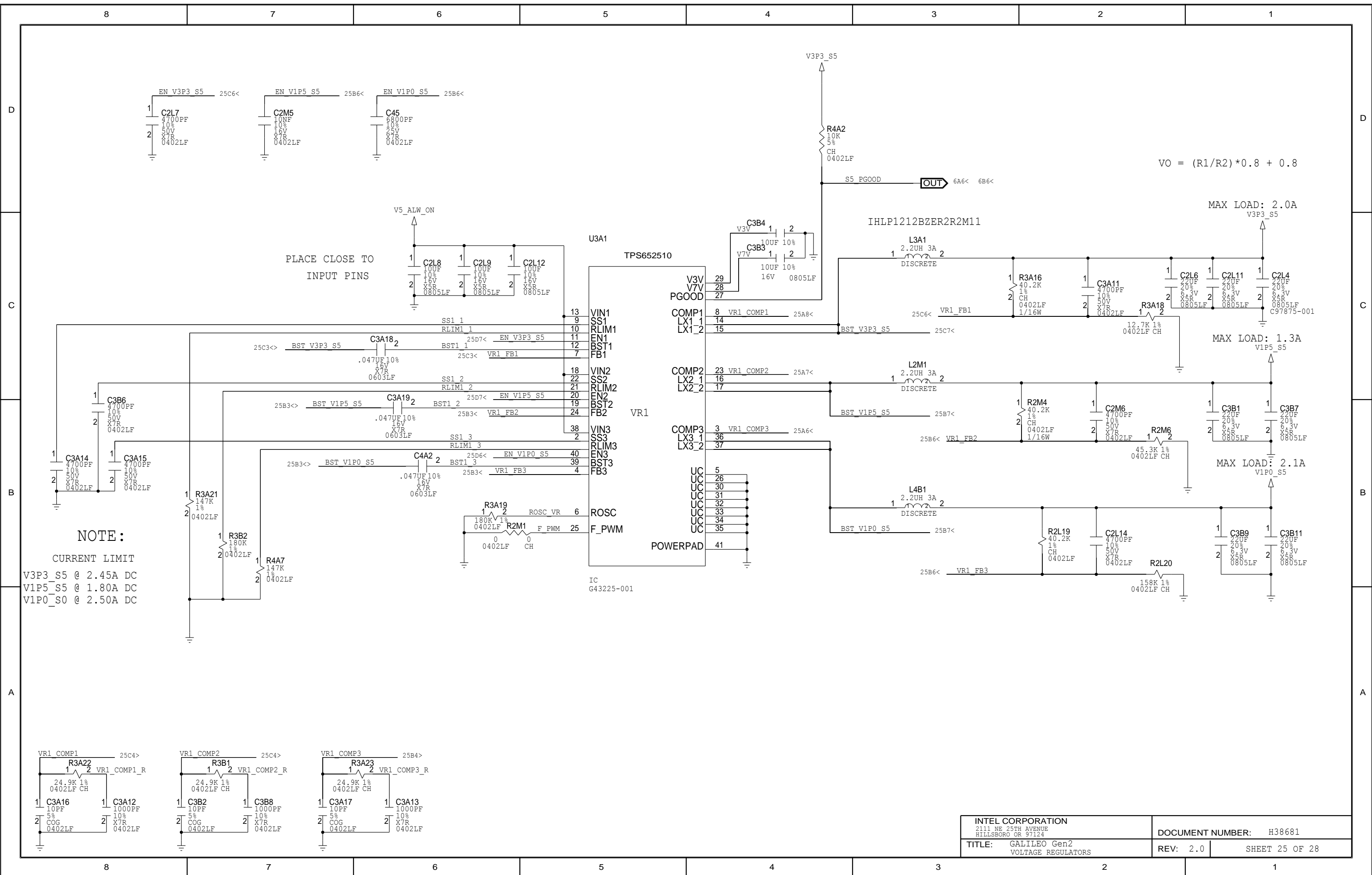






INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 LVL C BUFFER		REV: 2.0	SHEET 23 OF 28





PLACE CLOSE TO INPUT PINS

$$VO = (R1/R2) * 0.8 + 0.8$$

MAX LOAD: 2.0A

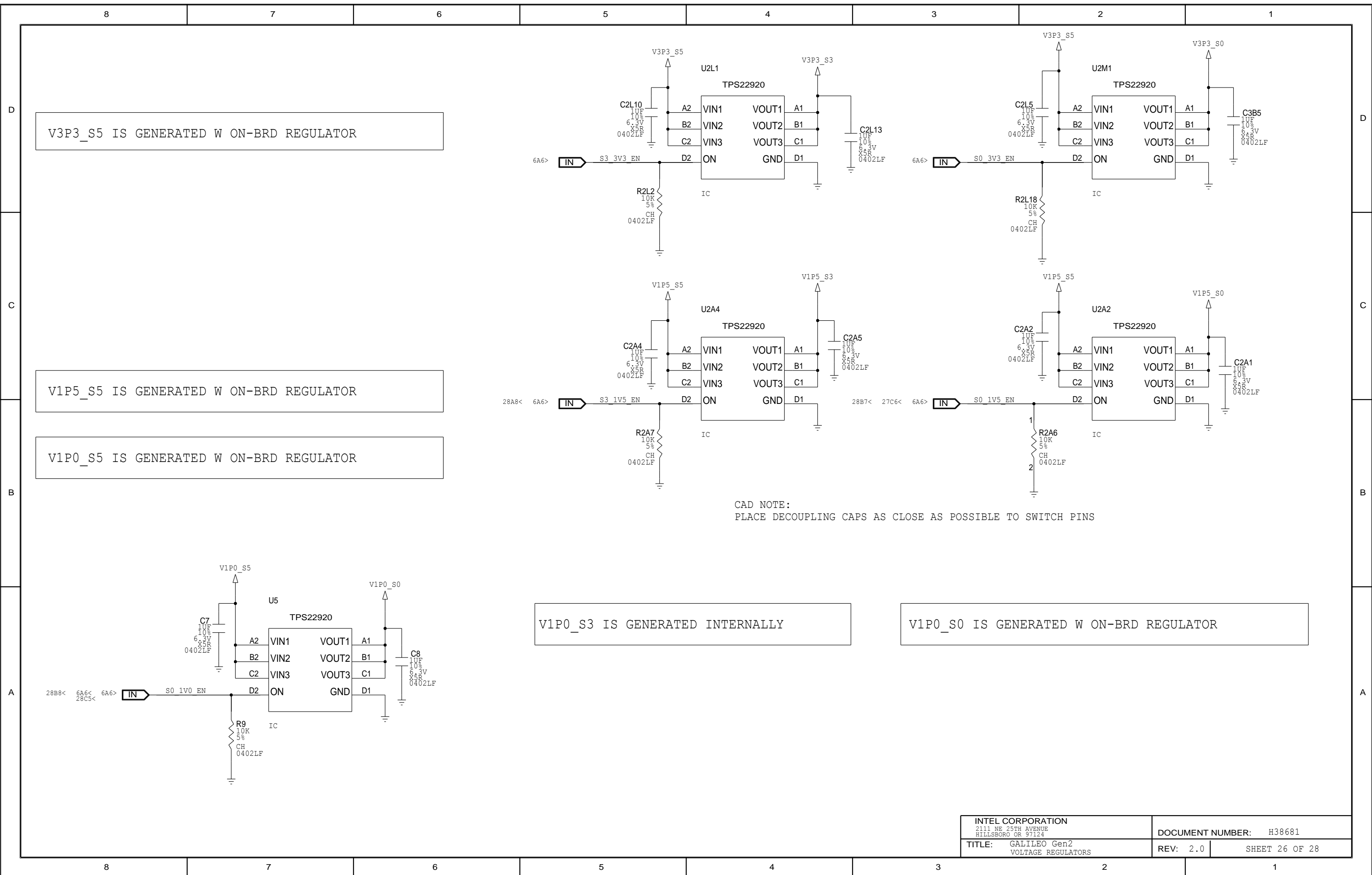
MAX LOAD: 1.3A

MAX LOAD: 2.1A

NOTE:

- CURRENT LIMIT
- V3P3_S5 @ 2.45A DC
- V1P5_S5 @ 1.80A DC
- V1P0_S0 @ 2.50A DC

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 VOLTAGE REGULATORS		REV: 2.0	SHEET 25 OF 28



V3P3_S5 IS GENERATED W ON-BRD REGULATOR

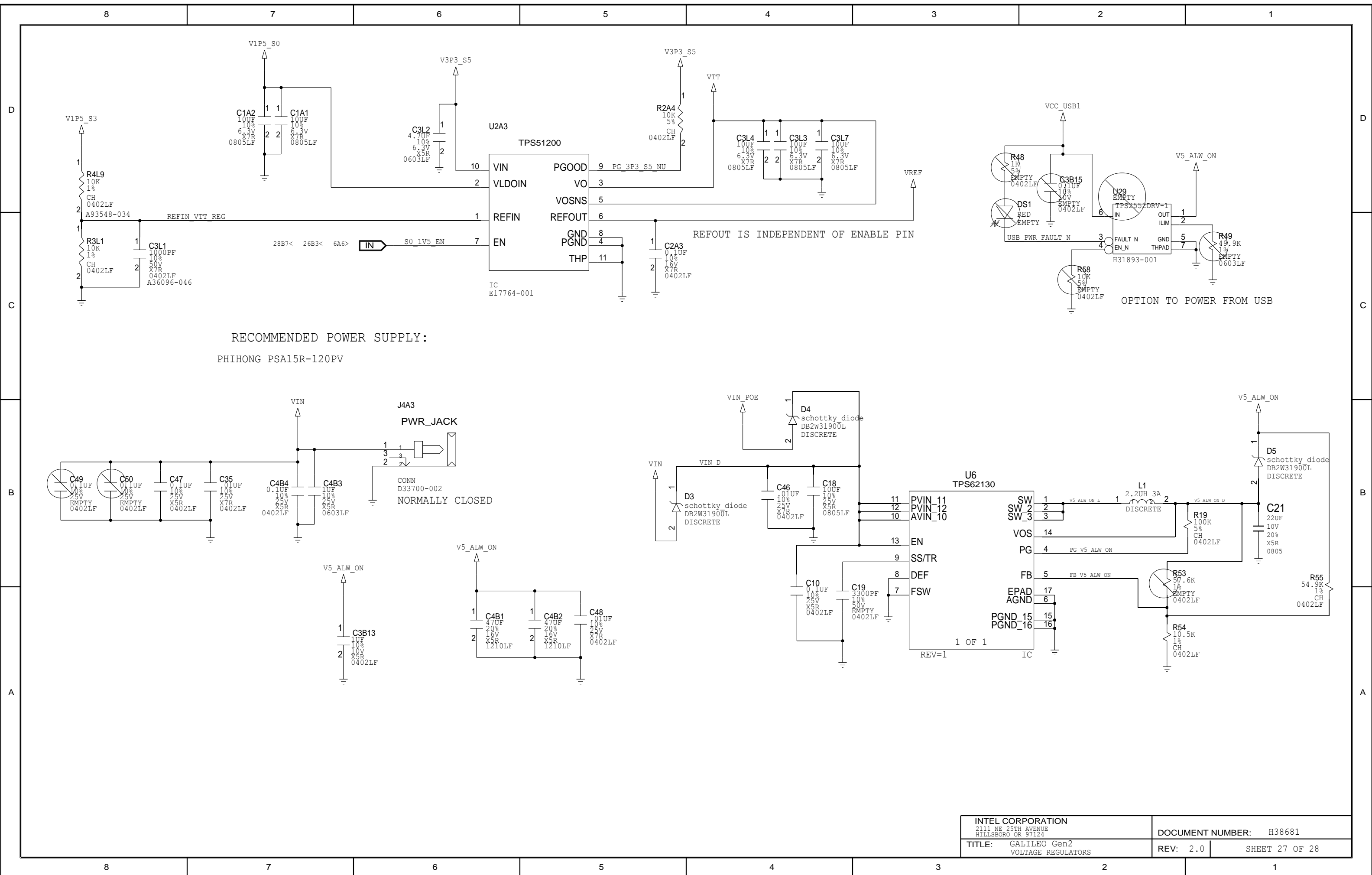
V1P5_S5 IS GENERATED W ON-BRD REGULATOR

V1P0_S5 IS GENERATED W ON-BRD REGULATOR

V1P0_S3 IS GENERATED INTERNALLY

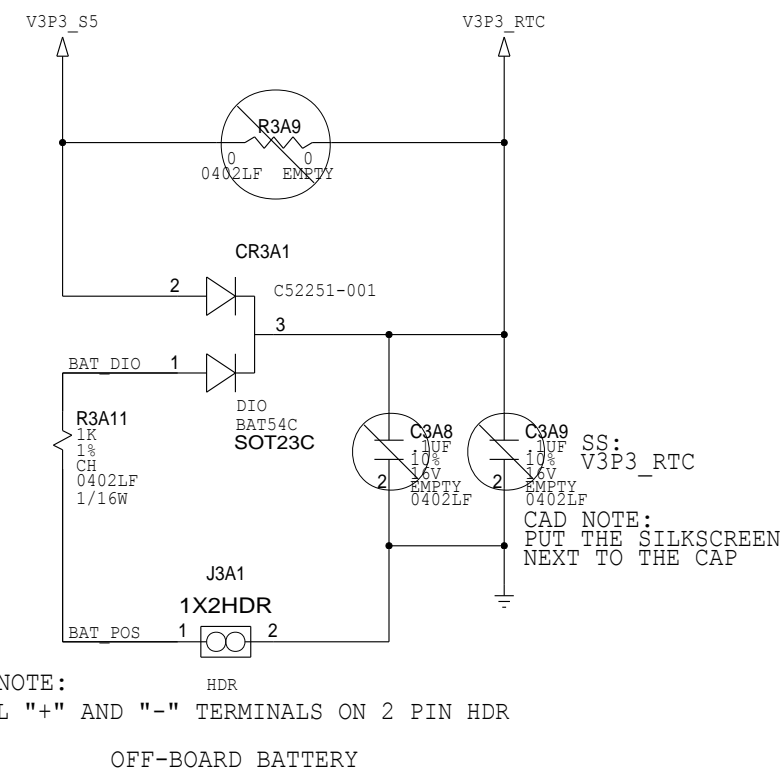
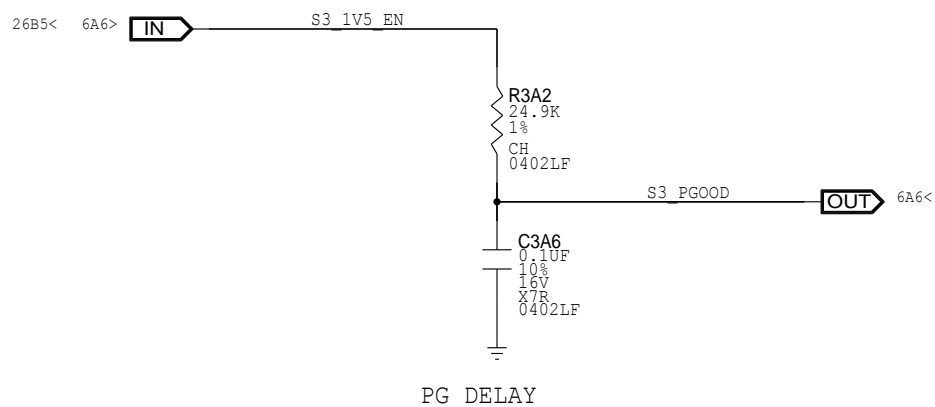
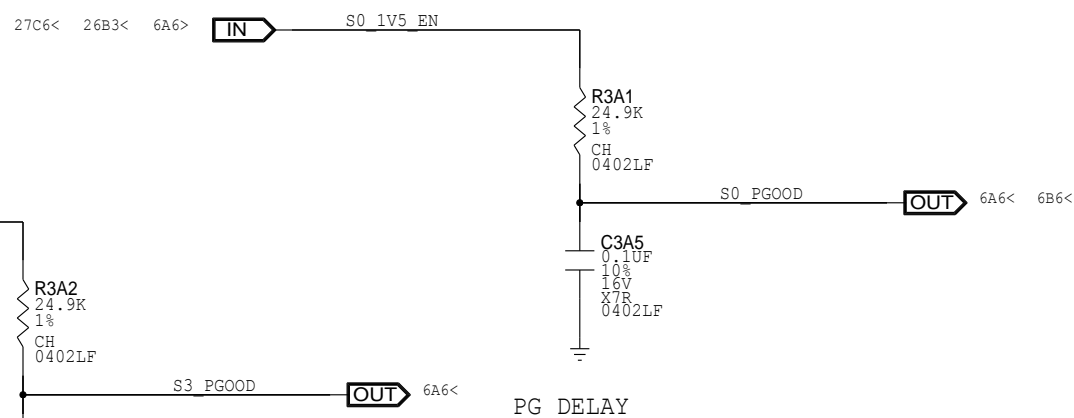
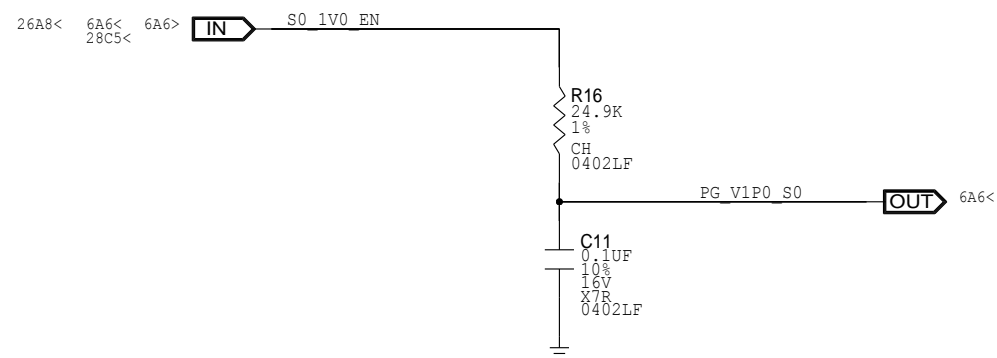
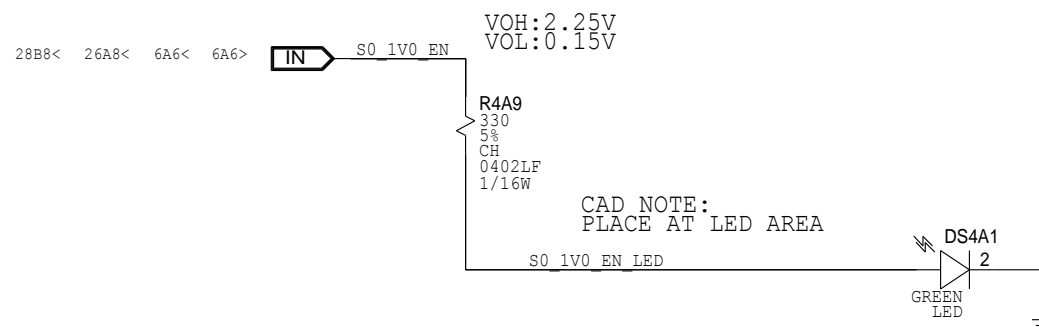
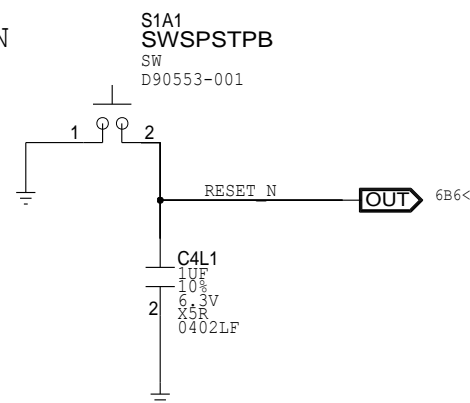
V1P0_S0 IS GENERATED W ON-BRD REGULATOR

CAD NOTE:
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS



NOTE: RESET_N HAS AN INTERNAL PU TO V3P3_S3

SS:
REBOOT BUTTON



CAD NOTE:
LABEL "+" AND "-" TERMINALS ON 2 PIN HDR
OFF-BOARD BATTERY

INTEL CORPORATION 2111 NE 25TH AVENUE HILLSBORO OR 97124		DOCUMENT NUMBER: H38681	
TITLE: GALILEO Gen2 POWER BUTTONS & MISC		REV: 2.0	SHEET 28 OF 28