GALILEO GEN2
INTEL QUARK X1000

FAB H
PB: H48142-207
PBA: H48125-800

INTEL CORPORATION

GALILEO Gen2
DESIGN TITLE PAGE

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STITCHING CAPS FOR SIGNAL REFERENCE TRANSITION

CAD NOTE
PLACE AS CLOSE AS POSSIBLE TO SIGNAL VIAS

STITCHING CAPS FOR SPLIT PLANES
CAD NOTE:
PLACE 0.1UF DECOUPLING AS CLOSE AS POSSIBLE TO DRAM POWER PINS

DESIGN NOTE:
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH 2GBIT(256MBIT X 8) AND 4GBIT (512MBIT X 8) DEVICES

SDRAM 1
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH SDRAM 2

CAD: PLACE 0.1UF DECOUPLING AS CLOSE AS POSSIBLE TO DRAM PINS

2GBIT(256MBIT X 8) AND 4GBIT (512MBIT X8) DEVICES

DESIGN NOTE:
A14, A15 ALLOW FOOTPRINT COMPATIBILITY WITH
2GBIT(256MBIT X 8) AND 4GBIT (512MBIT X8) DEVICES
Distribute Decoupling Among Termination Resistors
PCIE SLOT 0

**DYNAMIC CLK MANAGEMENT OUTPUT IS NOT SUPPORTED ON GALILEO**

**RESERVED PINS, NO CONNECT**

**NOT SUPPORTED BY QUARK**

**USER IDENTITY MODULE (EXTENSION OF SIM) NOT SUPPORTED BY QUARK**
CAD NOTE: PLACE SD LED CLOSE TO THE SDIO CONN
CAD NOTE:
PLACE CHOKE AND DIODES CLOSE TO USB CONN

NOTE:
PLACE C2B11 AS CLOSE AS POSSIBLE TO U3B1 PIN5
CAD NOTE:
PLACE CONNECTOR ON SOLDER-SIDE.
LSPI CS N HAS INTERNAL 20K FU IN QUARK

CAD NOTE:
PLACE DECOUPLING CAPACITORS AS CLOSE AS POSSIBLE TO ADC

BIOS STORAGE
(LOW) PUNIT BASE ADDRESS

(LOW) MEMORY DOWN CONFIG

(LOW) SINGLE RANK DDR3 SDRAM

(LOW) POWER BUTTON NOT USED

00 - REMOVABLE CARD SLOT FOR SDIO

01 - 1GBIT SDRAM

000 - QUARK SKU SETTINGS

(HIGH) X8 DDR SDRAM

DESIGN NOTE:
SHORT TO GND TO ENTER RECOVERY MODE.

SILK=FMR

RECOVERY MODE.

V3P3_S0

BIT1 BIT0

00 - REMOVABLE CARD SLOT FOR SDIO

BIT2

000 - QUARK SKU SETTINGS

01 - 1GBIT SDRAM

(SILK=FMR)

RECOVERY MODE.

V3P3_S0

BIT1 BIT0

00 - REMOVABLE CARD SLOT FOR SDIO

BIT2

000 - QUARK SKU SETTINGS

01 - 1GBIT SDRAM

(SILK=FMR)

RECOVERY MODE.
V1P0_S5 IS GENERATED W ON-BRD REGULATOR

V1P5_S5 IS GENERATED W ON-BRD REGULATOR

V1P0_S5 IS GENERATED W ON-BRD REGULATOR

V3P3_S5 IS GENERATED W ON-BRD REGULATOR

CAD NOTE:
PLACE DECOUPLING CAPS AS CLOSE AS POSSIBLE TO SWITCH PINS

V3P3_S0 IS GENERATED INTERNALLY

V1P5_S0 IS GENERATED W ON-BRD REGULATOR

V1P0_S3 IS GENERATED INTERNALLY

V1P0_S0 IS GENERATED W ON-BRD REGULATOR
RECOMMENDED POWER SUPPLY:

PHIHONG PSA15R-120PV

OPTION TO POWER FROM USB
NOTE: RESET_N HAS AN INTERNAL PU TO V3P3_S3